PT20

SDI/HD-SDI/3G-SDI Encoder

User Manual

Revision 1.1
7th January 2020

Revisions

Date	Revisions	Version
02-06-2019	First draft.	0.1
08-06-2019	Table 3 updated.	0.2
25-06-2019	SDI output modified. SMPTE-425M advanced formats added. PT20 pinouts updated. SDI output schematic added.	0.3
10-08-2019	SDI TI output removed. Clock2x input added. Hardware platform chapter added.	0.4
23-08-2019	Manual merged with PT21 user manual. Output TI device updated to LMH0340. PT6 details added. Test bench chapter updated. PT20 HD TRS input formats removed. BT656 input added. HPhase and VPhase controls added.	0.5
02-09-2019	PT21 description completed.	0.6
06-09-2019	Test bench chapter updated.	0.7
05-11-2019	More video standards added. Video standard input increased to 6 bits.	0.8
20-11-2019	PT20 manual separated from combined manual. Video standard input increased to 7 bits. Video standards reordered. Clock select outputs added. Clock valid input added. 50MHz clock input added. Video clock control added.	0.9
30-11-2019	Corrections to video standard table. (Table 4.) Input format table updated. (Table 3.) Added 2048x1080 standard. Hardware evaluation platform changed (to SM02). Text corrections.	1.0
07-01-2020	Corrections to Table 4. Payload inserted. Video input format assignments changed. 'Input select' port name changed to 'Format_select'. Test bench description moved to separate document.	1.1

Contents

Tables

Figures

1. Introduction

PT20 is an SDI/HD-SDI/3G-SDI encoder IP core.

PT20 accepts 8/10-bit BT656 format video (525i/625i operation) or 16/20-bit and 24/30/36-bit BT1120 format video with separate syncs (HD operation). SMPTE-425M advanced modes (4:4:4:4 RGB and 12-bit), are also accepted. PT20 encodes this data to a 20-bit data + clock output format for serializing in an external PHY.

PT20 comprises a single Verilog-2001 module. Table 1 shows the resources for the PT20 when compiled for an Altera (Intel) EP4CE15 FPGA. 643 logic elements are approximately equivalent to 9000 2-input NAND gates.

Logic Elements	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers
643	0	0	0	0

Table 1 PT20 Altera FPGA resource requirements.

2. PT20 Signal Interconnections

The PT20 signal interconnect diagram is shown in Figure 1.

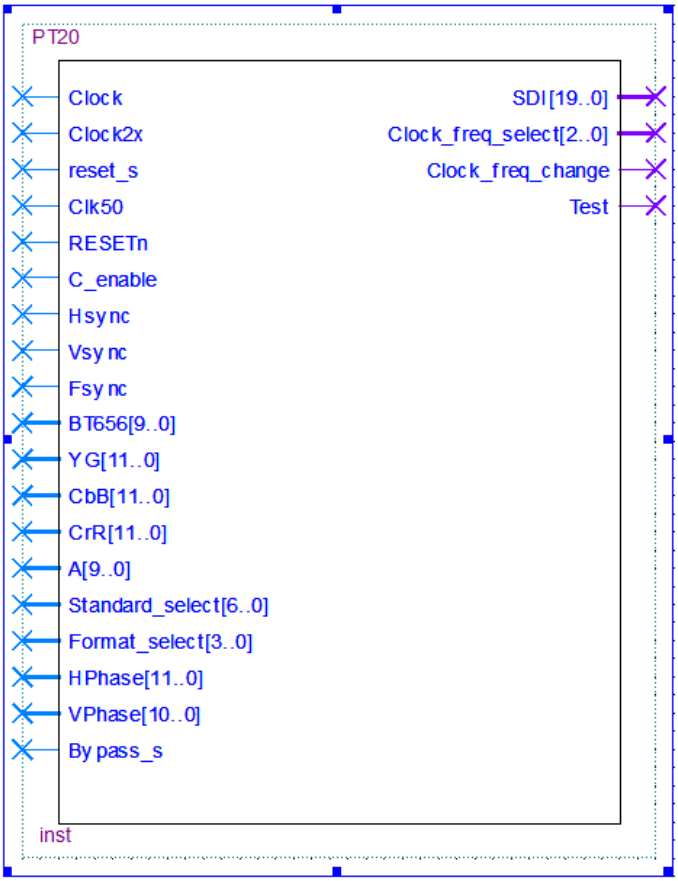

Figure 1 PT20 Block symbol.

The signal descriptions are shown in Table 2, below.

Inputs	
Signal	**Description**
Clock	Video clock input (13.5MHz for 525i/625i, 74.25MHz[1] for HD-SDI, 148.5MHz[2] for 3G-SDI). All data and sync inputs should be valid at the rising edge of this clock and the outputs are also valid at the rising edge of the clock. (See Table 3.)
Clock2x	27MHz clock input. This clock is only used for video format == 3'b000 for the demultiplexing of the BT656 input.
reset_s	Synchronous reset input. Connected to the PLL clock valid output to ensure initialization of counters when the video standard changes. See Chapter 4.
Clk50	Fixed 50MHz clock used for the video standard and clock control function. See Chapter 4.
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all registers.
C_enable	Used for demultiplexing the 4:2:2 16/20-bit input (Format_select = 4'b0001) or enabling the Cb/Cr input in 4:2:2 mode (Format_select = 3'b0010). When C_enable = '1'

	the Cb/Cr input is assumed to be Cb data, when '0' Cr data.
HSync	Active low horizontal sync input. The falling edge of this input is used to determine the output horizontal TRS position. For BT656 inputs this input should be tied low.
VSync	Active low vertical sync input. The falling edge of this input is used to determine the vertical TRS position (for non-interlaced inputs). For BT656 inputs this input should be tied low.
FSync	Active low vertical frame sync input (interlaced formats only). The high to low transition of this input determines field 1 of the interlaced frame. For BT656 inputs and non-interlaced formats this input should be tied low.
BT656[9:0]	BT656 input to the encoder. The input is straight binary, blanking level is 64_{10} and peak level 960_{10}. The BT656 input should be valid at the rising edge of 'Clock2x'. BT656[9] is the MSB. If the input is 8-bits wide, the bottom 2 bits should be tied to '0'.
YG[11:0]	Y (luma) input or G (green) input to the encoder. If Y or G, the input is straight binary, blanking level is 64_{10} and peak level 960_{10}. The Y input should be valid at the rising edge of 'Clock'. Unused bits should be tied to '0'.
CbB_in[11:0]	CbB (B-Y chroma) input or Cb/Cr multiplexed input or B (blue) input to the encoder. The Cb, Cb/Cr input is offset binary, blanking level is 512_{10}. The B input is straight binary. The data input should be valid at the rising edge of 'Clock'. Unused bits should be tied to '0'.
CrR_in[11:0]	CrR (R-Y chroma) input or R (red) input to the encoder. The Cr input is offset binary, blanking level is 512_{10}. The B input is straight binary. The data input should be valid at the rising edge of 'Clock'. Unused bits should be tied to '0'.
A[9:0]	Alpha channel input. The data input should be valid at the rising edge of 'Clock'. Unused bits should be tied to '0'.
Standard_select[6:0]	Selects the video standard being encoded (see Table 4).
Format_select[3:0]	Selects the video input format (see Table 3).
HPhase[11:0]	User controllable delay between the horizontal sync input and the insertion of SAV (Start of Active Video). HPhase is in units of 'Clock' cycles.
VPhase[10:0]	User controllable delay between the vertical sync input and the insertion of SAV vertical flag. VPhase is in units of 'HSync' lines.
Bypass_s	If Bypass_s = '1' the SMPTE scrambler and NRZI encoder are bypassed. Default setting should be '0'.
Outputs	
Signal	**Description**
SDI[19:0]	SDI output to PHY (see Chapter 4).
Clock_freq_select[2:0]	Output to PLL to select Clock and Clock2x frequency. See Chapter 4.
Clock_freq_change	Output to PLL to indicate when clock frequency needs to be changed. See Chapter 4.

Table 2 PT20 Signal Descriptions.

[1] For 29.97Hz and 59.94Hz field rates (HD) the clock is 74.17582418MHz (74.25MHz/1.001).
[2] For 29.97Hz and 59.94Hz field rates (HD) the clock is 148.35164836MHz (148.5MHz/1.001).

The Verilog instantiation of PT20 is shown below:

```
PT20 PT20_inst
(
.Clock(Clock_sig) ,                          // input  Clock_sig
.Clock2x(Clock2x_sig) ,                      // input  Clock2x_sig
.reset_s(reset_s_sig) ,                      // input  reset_s_sig
.Clk50(Clk50_sig) ,                          // input  Clk50_sig
.RESETn(RESETn_sig) ,                        // input  RESETn_sig
.C_enable(C_enable_sig) ,                    // input  C_enable_sig
.Hsync(Hsync_sig) ,                          // input  Hsync_sig
.Vsync(Vsync_sig) ,                          // input  Vsync_sig
.Fsync(Fsync_sig) ,                          // input  Fsync_sig
.BT656(BT656_sig) ,                          // input [9:0] BT656_sig
.YG(YG_sig) ,                                // input [11:0] YG_sig
.CbB(CbB_sig) ,                              // input [11:0] CbB_sig
.CrR(CrR_sig) ,                              // input [11:0] CrR_sig
.A(A_sig) ,                                  // input [9:0] A_sig
.Standard_select(Standard_select_sig) ,      // input [6:0] Standard_select_sig
.Format_select(Format_select_sig) ,          // input [2:0] Format_select_sig
.HPhase(HPhase_sig) ,                        // input [11:0] HPhase_sig
.VPhase(VPhase_sig) ,                        // input [10:0] VPhase_sig
.Bypass_s(Bypass_s_sig) ,                    // input  Bypass_s_sig

.SDI(SDI_sig) ,                              // output [19:0] SDI_sig
.Clock_freq_select(Clock_freq_select_sig) ,  // output [2:0] Clock_freq_select_sig
.Clock_freq_change(Clock_freq_change_sig)    // output  Clock_freq_change_sig
);
```

3. PT20 Technical Overview

A simplified block diagram of the PT20 is shown in Figure 2.

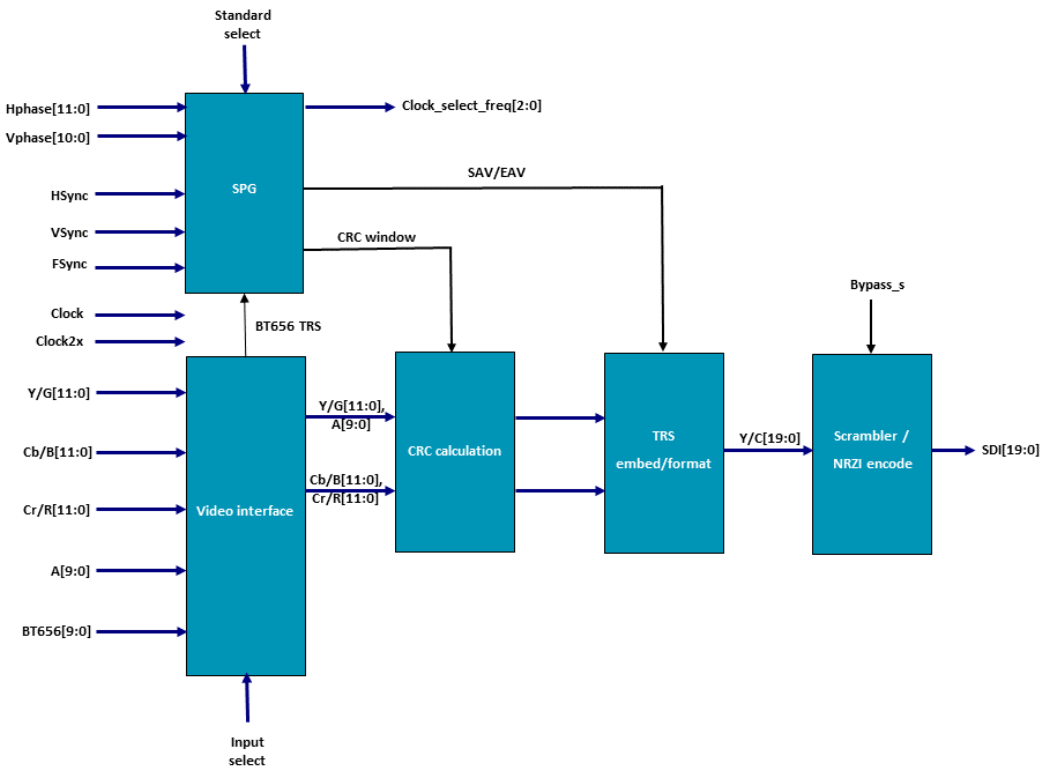

Figure 2 PT20 Block diagram.

The PT20 can accept 6 different formats of video/sync inputs as described in Table 3. Selection of the input format is made using Format_select[3:0] bits.

Format select[3:0]	BT656[9:0]	YG[11:0]	CbB[11:0]	CrR[11:0]	A[9:0]	Comments
0000	BT656 input[9:0] (10-bit) or BT656[9:2] (8-bit).	Not used	Not used	Not used.	Not used.	(SMPTE-425M mapping 1.) Multiplexed 4:2:2 Y/Cb/Cr inputs (8/10-bits). BT656 input is clocked with 'Clock2x'. Synchronising inputs are extracted from the BT656 input (TRS). Unused inputs should be set to '0'.
0001	Not used	Y input[9:0] (10-bit) or Y input [9:2] (8-bit).	Cb/Cr input[9:0] (10-bit) or Cb/Cr input [9:2] (8-bit).	Not used.	Not used.	(SMPTE-425M mapping 1.) Separate Y and multiplexed Cb/Cr 4:2:2 inputs (16/20-bits). Y data is clocked with 'Clock'; Cb/Cr data are clocked with 'Clock' with 'C_enable' signaling which is Cb (= '1') or Cr (= '0'). Synchronising inputs are HSync_in, VSync_in and FSync_in (if interlaced). Unused inputs should be set to '0'.
0010	Not used	Y input[9:0] (10-bit) or Y input [9:2] (8-	Cb input[9:0] (10-bit) or	Cr input[9:0] (10-bit) or	Not used.	(SMPTE-425M mapping 1.) Separate Y/Cb/Cr inputs (24/30-bits, 4:2:2 mode). Y

Format select[3:0]	BT656[9:0]	YG[11:0]	CbB[11:0]	CrR[11:0]	A[9:0]	Comments
		bit).	Cb input [9:2] (8-bit).	Cr input [9:2] (8-bit).		data is clocked with 'Clock'; Cb/Cr data are clocked with 'Clock' if 'C_enable' is '1'. Synchronising inputs are HSync_in, VSync_in and FSync_in (if interlaced video). Unused inputs should be set to '0'.
0100	Not used	Y (luma) input[9:0] (10-bit).	Cb (B-Y) input[9:0] (10-bit).	Cr (R-Y) input[9:0] (10-bit).	Not used.	(SMPTE-425M mapping 2). Separate YCbCr inputs (4:4:4). YCbCr data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'.
0101	Not used	G (green) input[9:0] (10-bit).	B (Blue) input[9:0] (10-bit).	R (Red) input[9:0] (10-bit).	Not used.	(SMPTE-425M mapping 2). Separate RGB inputs (4:4:4). RGB data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'.
0110	Not used	Y (luma) input[9:0] (10-bit).	Cb (B-Y) input[9:0] (10-bit).	Cr (R-Y) input[9:0] (10-bit).	A[9:0].	(SMPTE-425M mapping 2). Separate YCbCrA inputs (4:4:4:4). YCbCrA data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'. The A channel should be video information.
0111	Not used	G (green) input[9:0] (10-bit).	B (Blue) input[9:0] (10-bit).	R (Red) input[9:0] (10-bit).	A[9:0].	(SMPTE-425M mapping 2). Separate RGBA inputs (4:4:4:4). RGB data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'. The A channel should be video information.
1000	Not used	Y (luma) input[9:0] (10-bit).	Cb (B-Y) input[9:0] (10-bit).	Cr (R-Y) input[9:0] (10-bit).	A[9:2].	(SMPTE-425M mapping 2). Separate YCbCrA inputs (4:4:4:4). YCbCrA data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'. The A channel should be data information.
1001	Not used	G (green) input[9:0] (10-bit).	B (Blue) input[9:0] (10-bit).	R (Red) input[9:0] (10-bit).	A[9:2].	(SMPTE-425M mapping 2). Separate RGBA inputs (4:4:4:4). RGB data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in. Unused inputs should be set to '0'. The A channel should be data information.
1010	Not used	Y (luma) input[11:0] (12-bit)	Cb (B-Y) input[11:0] (12-bit)	Cr (R-Y) input[11:0] (12-bit)	Not used.	(SMPTE-425M mapping 3). Separate YCbCr inputs (36-bits, 4:4:4). Video data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in.
1011	Not used	G (green)	B (Blue)	R (Red)	Not used.	(SMPTE-425M mapping 3).

Format select[3:0]	BT656[9:0]	YG[11:0]	CbB[11:0]	CrR[11:0]	A[9:0]	Comments
		input[11:0] (12-bit)	input[11:0] (12-bit)	input[11:0] (12-bit)		Separate RGB inputs (36-bits, 4:4:4). Video data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in.
1100	Not used	Y (luma) input[11:0] (12-bit)	Cb (B-Y) input[11:0] (12-bit)	Cr (R-Y) input[11:0] (12-bit)	Not used.	(SMPTE-425M mapping 4). Separate YCbCr inputs (36-bits, 4:2:2). Video data is clocked with 'Clock'; Synchronising inputs are HSync_in, VSync_in and FSync_in.

Table 3 PT20 Input video formats.

For 525i and 625i SD video standards the BT656 input may be used (Format_select = 4'b0000). The BT656 input is decoded to detect the TRS (Timing Reference Signal) pulses and demultiplexed into its sync and video components. Horizontal and vertical syncs are generated from the decoded TRS.

For HD video standards the separate HSync/VSync and FSync inputs should be used. The SPG (sync pulse generator) generates horizontal (pixel) and vertical (line) counts synchronized to the regenerated BT656 syncs or the separate syncs.

From the horizontal sync input, the output SAV (Start of Active Video) and EAV (End of Active Video) codes are generated (see Figure 3). From the falling edge of the regenerated horizontal sync a fixed delay, dependent on the video standard is added to a user controllable offset (HPhase[11:0]) before the SAV code is inserted into the SDI output. The EAV code is inserted after the active picture period as shown in Table 4.
The HPhase value will 'wrap' at the (total line length – 1) as shown in Table 4. For example, for 720p/60, HPhase will wrap at 1650 – 1 = 1649. To delay the TRS insertion Hphase should be increased in value to a maximum value of 1649. To shift the TRS insertion forward HPhase should be reduced from maximum value 1649.

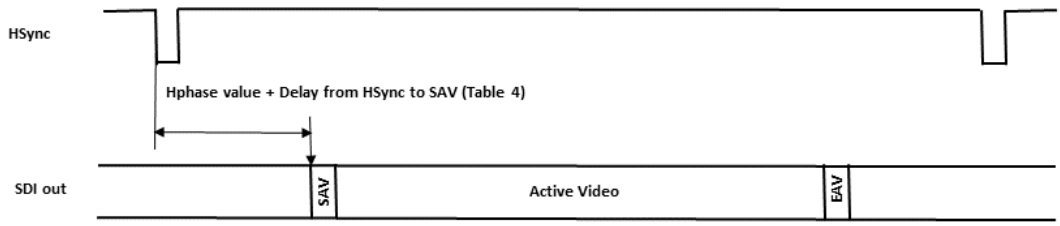

Figure 3 Horizontal sync timing.

From the vertical sync input (either VSync or FSync for HD video or the recovered FSync from the BT656 input for SD video) a regenerated vertical sync pulse is created, VPhase lines delayed from the falling edge of the VSync or FSync input. If VPhase is set to zero the falling edge of the VSync or FSync input is line 1 for the SDI output.
The VPhase value will 'wrap' at the (total lines/frame – 1) as shown in Table 5. For example, for 720p/60, VPhase will wrap at 750 – 1 = 749. To increase line value number for HD or the position of the VFlag and FFlag for SD, the Vphase should be increased in value to a maximum value of 749. To shift the decrease the line value number VPhase should be reduced from maximum value 749.

The SPG generates the SAV and EAV (end of active video) sync pulses and the vertical flag (and frame ID for interlaced standards), forming them into a Hamming word for inclusion in the final TRS code. The SPG also generates the line count value for the HD-SDI/3G-SDI standards and embeds the Cyclic Redundancy Check (CRC) sum. The CRC sum is calculated during the active video using the polynomial $X^{18} + X^5 + X^4 + 1$.

The format of the TRS codes for SD and HD video are shown in Figure 4.

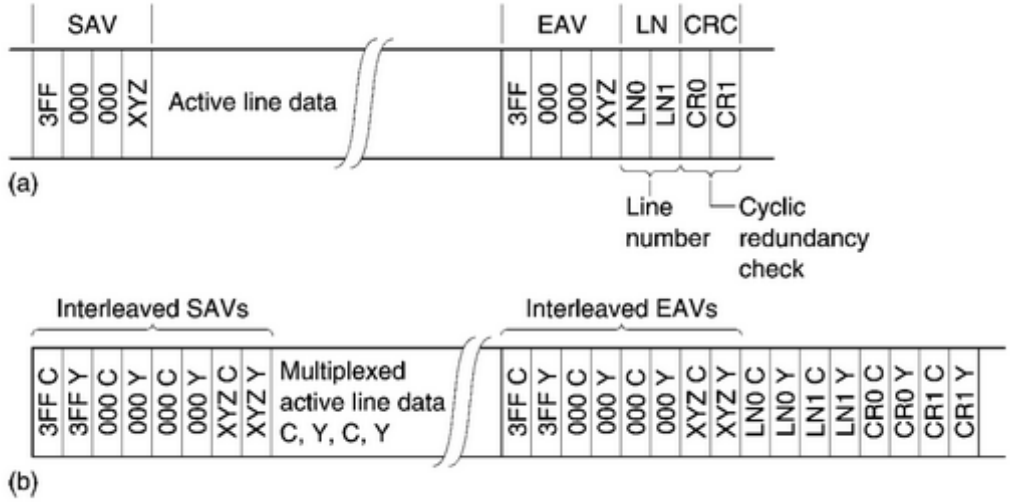

Figure 4 TRS structure (a) SD and (b) HD.

Standard Select[6:0]		Standard	Lines/frame	SMPTE standard	Clock	Pixels/line	Active Line period (pixels)	Format_select (Table 3)
0000000	0	525i/59.94Hz	525	SMPTE-259M	27.0MHz	1716	1440	'0000', '0001' or '0010' (SMPTE-425 mapping 1).
0000001	1	625i/50Hz	625		27.0MHz	1728	1440	
0010000	16	720p/23.98Hz	750	SMPTE-292M	74.18MHz	4125	1280	'0001' or '0010' (SMPTE-425 mapping 1).
0010001	17	720p/24Hz	750		74.25MHz	4125	1280	
0010010	18	720p/25Hz	750		74.25MHz	3960	1280	
0010011	19	720p/29.97Hz	750		74.18MHz	3300	1280	
0010100	20	720p/30Hz	750		74.25MHz	3300	1280	
0010101	21	720p/50Hz	750		74.25MHz	1980	1280	
0010110	22	720p/59.97Hz	750		74.18MHz	1650	1280	
0010111	23	720p/60Hz	750		74.25MHz	1650	1280	
0011000	24	1080p/23.98Hz	1125		74.18MHz	2750	1920	
0011000	25	1080p/24Hz	1125		74.25MHz	2750	1920	
0011001	26	1080p/25Hz	1125		74.25MHz	2640	1920	
0011010	27	1080p/29.97Hz	1125		74.18MHz	2200	1920	
0011011	28	1080p/30Hz	1125		74.25MHz	2200	1920	
0011100	29	1080i/50Hz	1125		74.25MHz	2640	1920	
0011101	30	1080i/59.94Hz	1125		74.18MHz	2200	1920	
0011110	31	1080i/60Hz	1125		74.25MHz	2200	1920	
0100000	32	1035i/29.97	1125	SMPTE-260M	74.18MHz	2200	1920	'0001' or '0010' (SMPTE-425 mapping 1).
0100001	33	1035i/30	1125		74.25MHz	2200	1920	
1000000	64	720p/23.98Hz	750	SMPTE-425M	148.35MHz	4125	1280	'0100', '0101', '0110', '0111', '1000' or '1001'. (SMPTE-425 mapping 2).
1000001	65	720p/24Hz	750		148.5MHz	4125	1280	
1000010	66	720p/25Hz	750		148.5MHz	3960	1280	
1000011	67	720p/29.97Hz	750		148.35MHz	3300	1280	
1000100	68	720p/30Hz	750		148.5MHz	3300	1280	
1000101	69	720p/50Hz	750		148.5MHz	1980	1280	
1000110	70	720p/59.94Hz	750		148.35MHz	1650	1280	
1000111	71	720p/60Hz	750		148.5MHz	1650	1280	
1001000	72	1080p/23.98Hz	1125		148.35MHz	2750	1920	'0100', '0101', '0110', '0111' '1000', '1001', '1010', '1011', or '1100'. (SMPTE-425 mapping 2, 3 or 4).
1001001	73	1080p/24Hz	1125		148.5MHz	2750	1920	
1001010	74	1080p/25Hz	1125		148.5MHz	2640	1920	
1001011	75	1080p/29.97Hz	1125		148.35MHz	2200	1920	
1001100	76	1080p/30Hz	1125		148.5MHz	2200	1920	
1001101	77	1080i/50Hz	1125		148.5MHz	2640	1920	
1001110	78	1080i/59.94Hz	1125		148.35MHz	2200	1920	
1001111	79	1080i/60Hz	1125		148.5MHz	2200	1920	
1010000	80	1080p/50Hz	1125		148.5MHz	2640	1920	'0001' or '0010' (SMPTE-425 mapping 1).
1010001	81	1080p/59.97Hz	1125		148.35MHz	2200	1920	
1010010	82	1080p/60Hz	1125		148.5MHz	2200	1920	
1010011	83	1080p/24Hz	1125	SMPTE-428	148.5MHz	2750	2048	'1010' or '1011'. (SMPTE-425 mapping 3).

Table 4 Supported video standards.

The chroma and luma channels of the video are then multiplexed at half clock rate according to the Format_select setting (e.g. 10-bit YCbCr or 12-bit RGB). The multiplexed video is then stripped of invalid codes (<4 or >1019 for 10 bit video). The formatted video then has the CRC (cyclic redundancy check) calculated for the Y and Cb/Cr channels. Based on the Input standard and the Format select inputs, the Payload is created (according to SMPTE-352M) and inserted on the specified line after the EAV.

The TRS word and the video data are multiplexed together into a single video stream. The video stream is then scrambled according using the polynomial $X^9 + X^4 + 1$ and then encoded to a 20-bit NRZI output. The block diagram of a single bit scrambler and NRZI encoder is shown in Figure 5. To avoid having to operate the scrambler at the final SDI clock rate, an equivalent multi-bit scrambler is used which operates at 'Clock' rate.

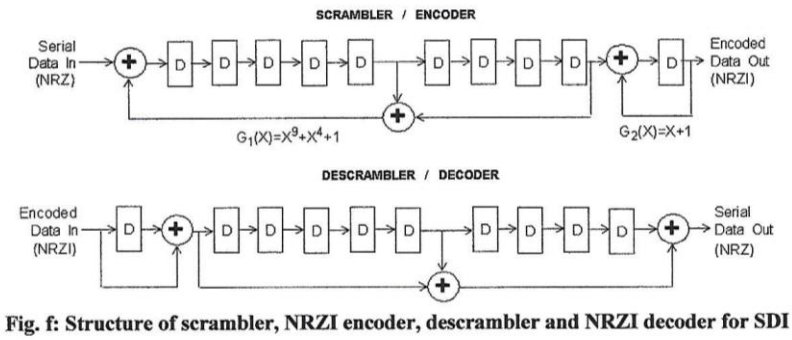

Figure 5 SMPTE scrambler/descrambler and NRZI encoder/decoder.

The format of the multiplexed output is described in Chapter 4.

4. PT20/PT21 PHY Interface

The PT20 provides a 20-bit SDI output.

SDI[19:0] is designed to interface to the Silicon Creations PMATS40LPDL1EB1 PHY IP core. The PT20 provides a 20-bit output at the 'Clock' data rate. The PHY should serialise this data, LSB first to the output data rate. For example, at a data clock rate of 74.25MHz, the output of the serialiser will be 74.25MHz x 20 bits = 1.485GHz.

To hardware test the PT20 prior to the final ASIC implementation the 20-bit SDI output is modified to allow it to drive a Texas Instruments (TI) LMH0340 serialiser. The 20-bit SDI_TI output should be serialized 4:1 in multiplexer. The LMH0040 series ICs require a 5-bit LVDS data input with a twice rate LVDS clock (both edges of the clock are used to serialise the data).

First the SDI[19:0] output has to be modified to match the input data sequence of the LMH0340.

```
// Remap data to LMH0340
   always @(posedge Clock) begin
     for (J = 0; J <= 4; J = J + 1) begin
     SDI_TI[3 + (4*J)] <= SDI[J]    ;
     SDI_TI[2 + (4*J)] <= SDI[J+5]  ;
     SDI_TI[1 + (4*J)] <= SDI[J+10] ;
     SDI_TI[0 + (4*J)] <= SDI[J+15] ;
     end
end
```

The 20-bit data is then 4:1 multiplexed into 5 data output streams. For this purpose, an Altera library function is used.

```
LVDS_Mux LVDS_Mux(.tx_in(SDI_TI[19:0]), .tx_inclock(Clock2x), .tx_syncclock(Clock),
                  .tx_out(LVDS_Tx[4:0]));
```

The 5 bit data and the associated clock is then converted to a differential LVDS output to drive the LMH0340.

```
LVDS_Tx    LVDS_Tx_Clk(.datain(LVDS_Tx_Clock2x), .dataout(TxClk_P), .dataout_b(TxClk_N));
LVDS_Tx    LVDS_Tx_Tx0(.datain(LVDS_Tx[0]), .dataout(Tx0_P), .dataout_b(Tx0_N));
LVDS_Tx    LVDS_Tx_Tx1(.datain(LVDS_Tx[1]), .dataout(Tx1_P), .dataout_b(Tx1_N));
LVDS_Tx    LVDS_Tx_Tx2(.datain(LVDS_Tx[2]), .dataout(Tx2_P), .dataout_b(Tx2_N));
LVDS_Tx    LVDS_Tx_Tx3(.datain(LVDS_Tx[3]), .dataout(Tx3_P), .dataout_b(Tx3_N));
LVDS_Tx    LVDS_Tx_Tx4(.datain(LVDS_Tx[4]), .dataout(Tx4_P), .dataout_b(Tx4_N));
```

The schematic for the LMH0340 is shown in Figure 6. The PT20 is compiled for an Altera EP4CE15E22I7N FPGA. An Altera library multiplexer is used to multiplex the SDI_TI 20-bit data to 5-bits and a PLL generates the twice-rate clock for the LMH0340 (note that the LVDS_Tx_Clock2x clock to the LMH0340 is shifted 90deg in phase to match the timing requirements of the LMH0340). The lock output LED indicates the LMH0340 PLL has locked. The SDI output from the LMH0040 is terminated and AC coupled to the output BNC connector. The 6.8nH inductor is to improve the return loss.

The hardware evaluation platform for the PT20 generates a 27MHz clock. This is multiplied in a fractional PLL (IDT MK2716) to either 74.25MHz or 74.18MHz (74.25MHz/1.001) which is chosen on the basis of the video standard selected. This clock is the then input to an Altera FPGA PLL which can be reconfigured to output either 27MHz for SDI, 74.25MHz for HD-SDI or twice that for 3G-SDI, 148.5MHz.

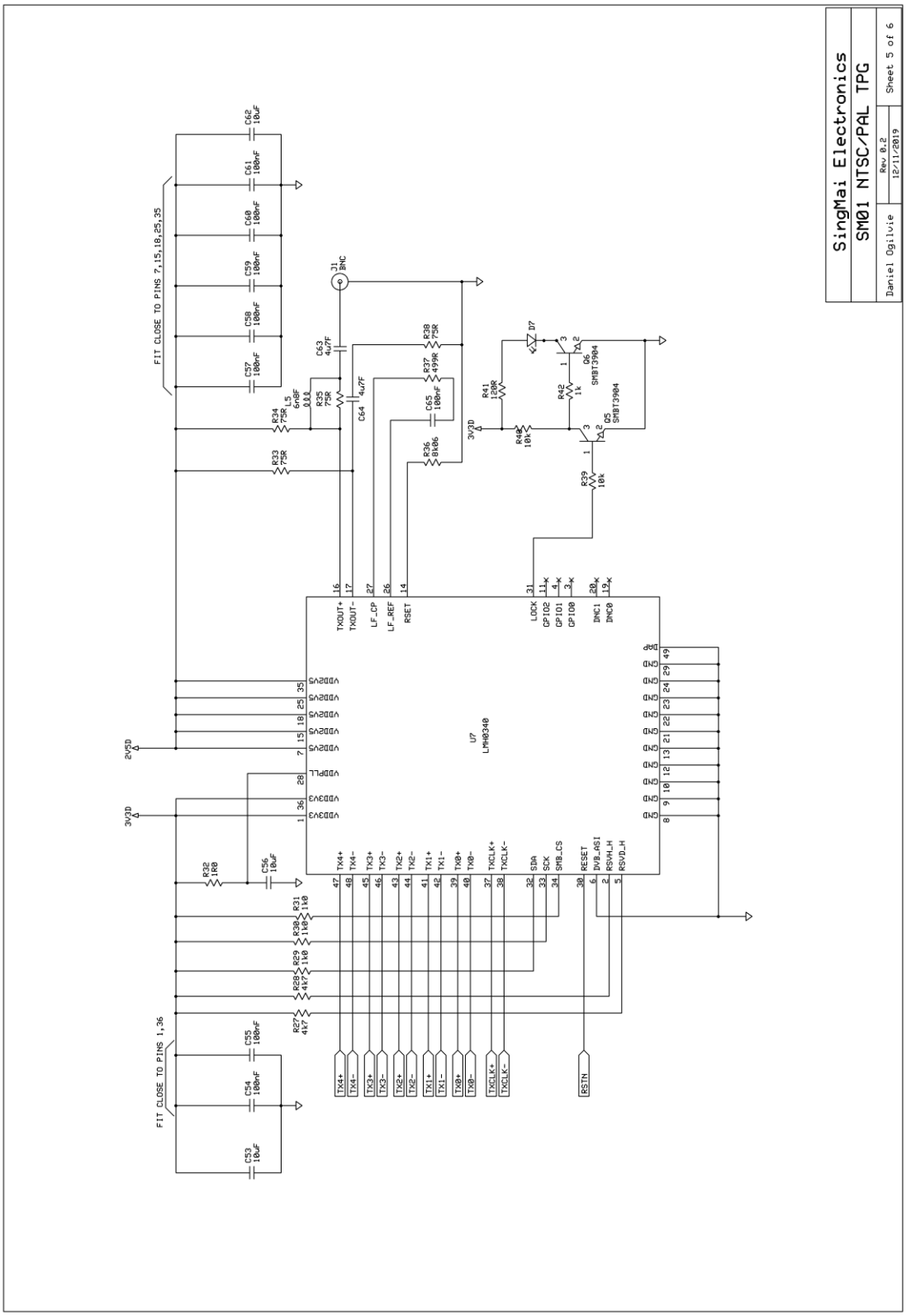

Figure 6 LMH0340 Tx schematic.

The PT20 controls the PLL which generates the Clock and Clock2x inputs to the PT20 (see Figure 7).

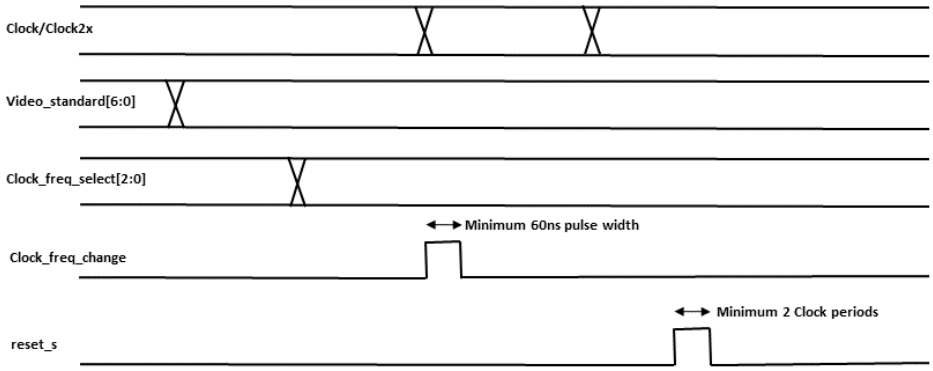

Figure 7 PT20 PLL control.

If the video standard input to the PT20 is changed and requires a different clock frequency, after a short delay the Clock_freq_select bits will change to select another clock (see Table 5).

Clock_freq_select[2:0]	Clock	Clock2x	Comment
000	13.5MHz	27MHz	
001	74.18MHz	148.35MHz	Clock = 74.25MHz/1.001
010	74.25MHz	148.5MHz	
011	148.35MHz	296.7MHz	Clock = 148.5MHz/1.001
100	148.5MHz	297MHz	
101-111	Not used	Not used	

Table 5 PLL frequencies.

Once the frequency select bits are stable a short pulse (Clock_freq_change) will indicate to the PLL that a clock change is necessary. After the PLL has changed the clock frequency and the clock is stable the PLL should strobe the reset_s input to the PT20. This will synchronously reset all the registers in the PT20 to ensure that any clock disturbance has not put a counter or state machine into an invalid state.

5. PT20 Test bench

The PT20 test bench description may be found in the document, 'PT20 PT21 Test Bench User manual 0.1'.