

Features

PLL generated (32 to 192 kHz) or direct master clock
Low EMI design
109 dB DAC/105 dB ADC Dynamic Range and SNR
-94 dB THD+N
Single 3.3V Supply
Tolerance for 5V logic inputs
Supports 24-bits and 8 kHz to 192 kHz sample rates
Differential ADC input
Single-ended or Differential DAC output versions
Log volume control with "auto-ramp" function
Software controllable clickless mute
Software power-down
Right justified, left justified, I²S and TDM Modes
Master and slave modes up to 16 channel in/out
48-lead LQFP or 64-lead LQFP plastic package

Applications

Consumer audio systems
Home theater systems
Set-top boxes
Digital audio effects processors

GENERAL DESCRIPTION

The ADAU132X family are high performance, single-chip codecs that provide 2 ADCs with differential input and 8 DACs with either single-ended or differential output using ADI's patented multibit sigma-delta architecture. An SPI® or I²C® port is included, allowing a microcontroller to adjust volume and many other parameters. The ADAU132X family operates from 3.3V digital and analog supplies. The ADAU132X is available in a 48-lead (SE output) or 64-lead (differential output) LQFP package.

The ADAU132X is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive master clock from L-R clock, the ADAU132X eliminates the need for a separate high frequency master clock. It can also be used with a suppressed bit clock. The D-A and A-D converters are designed using the latest ADI continuous time architectures to further minimize EMI. By using 3.3V supplies, power consumption is minimized, further reducing emissions.

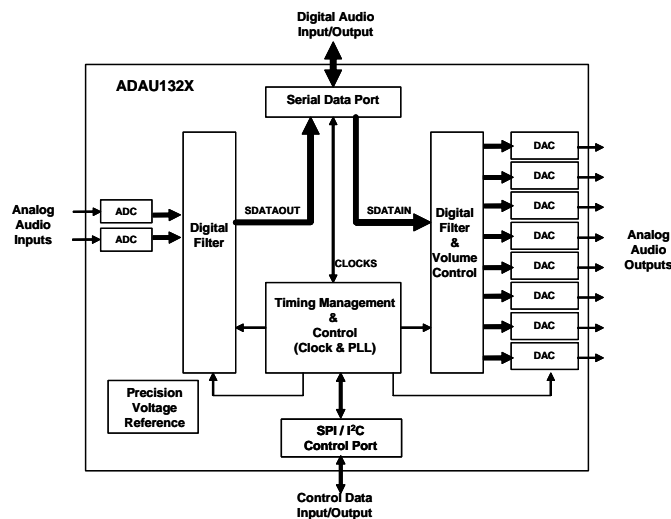
Functional Block Diagram


Figure 1

Rev. PrB September 14, 2005

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ADAU132X—SPECIFICATIONS

Test Conditions, Unless Otherwise Noted.

Performance of all channels is identical (exclusive of the Inter-channel Gain Mismatch and Inter-channel Phase Deviation specifications).

Parameter	Rating
Supply Voltages (AVDD, DVDD)	3.3 V
Case Temperature	25°C
Master Clock	12.288 MHz (48 kHz f_s , 256 × f_s Mode)
Input Signal	1.000 kHz, 0 dBFS (Full Scale), -1 dBVrms (0.9Vrms)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance (Digital Output)	50 pF
Load Current (Digital Output)	±1 mA or 1.5kΩ to ½ DVDD supply
Input Voltage HI	2.0 V
Input Voltage LO	0.8 V

Table 1

Analog Performance

Parameter	Min	Typ	Max	Unit	
ANALOG-TO-DIGITAL CONVERTERS	ADC Resolution (all ADCs)	24		Bits	
	Dynamic Range (20 Hz to 20 kHz, -60 dB Input) ¹				
	No Filter (RMS)		102		dB
	With A-Weighted Filter (RMS)		105		dB
	Total Harmonic Distortion + Noise (-1 dBFS) ¹		-98		dB
	Full-Scale Input Voltage (Differential)		2.0		V rms
	Gain Error	-7.0		+7.0	%
	Interchannel Gain Mismatch	-0.2		+0.2	dB
	Offset Error	-7	0	+7	mV
	Gain Drift		100		ppm/°C
	Interchannel Isolation		-110		dB
	CMRR, 100 mV RMS, 1 kHz		55		dB
	CMRR, 100 mV RMS, 20 kHz		55		dB
	Input Resistance		14		kΩ
	Input Capacitance		10		pF
Input Common-Mode Bias Voltage		1.5		V	
DIGITAL-TO-ANALOG CONVERTERS	Dynamic Range (20 Hz to 20 kHz, -60 dB Input) ¹				
	No Filter (RMS), Single-ended version		101		dB
	With A-Weighted Filter (RMS), Single-ended version		104		dB
	With A-Weighted Filter (Avg), Single-ended version		106		dB
	No Filter (RMS), Differential version		104		dB
	With A-Weighted Filter (RMS), Differential version		107		dB
	With A-Weighted Filter (Avg), Differential version		109		dB
	Total Harmonic Distortion + Noise (0 dBFS) ¹				
	Single-ended version		-90		dB
	Differential version		-92		dB
	Full-Scale Output Voltage (Single-ended version)		0.9 (2.5)		V rms (V pp)
	Full-Scale Output Voltage (Differential version)		1.8 (5.0)		V rms (V pp)
	Gain Error	-7%		+7%	%
Interchannel Gain Mismatch	-0.5		+0.5	dB	

¹Total harmonic distortion + noise and dynamic range typical specifications are for two channels active, max/min are all channels active.

Parameter	Min	Typ	Max	Unit
Offset Error, Single-ended version		-15		mV
Offset Error, Differential version		-10		mV
Gain Drift	-30		30	ppm/°C
Interchannel Isolation		100		dB
Interchannel Phase Deviation		0		Degrees
Volume Control Step		0.375		dB
Volume Control Range		95		dB
De-emphasis Gain Error			±0.6	dB
Output Resistance at Each Pin		100		Ω
REFERENCE	Internal Reference Voltage, FILTR	1.50		V
	External Reference Voltage, FILTR	1.50		V
	Common-Mode Reference Output, CM	1.50		V

Table 2

Crystal Oscillator

Parameter	Min	Typ	Max	Unit
Transconductance		3.5		mmhos

Table 3

Digital I/O

Parameter	Min	Typ	Max	Unit
Input Voltage HI (V _{IH})	2.0			V
Input Voltage LO (V _{IL})			0.8	V
Input Leakage (I _{IH} @ V _{IH} = 2.4 V)			10	μA
Input Leakage (I _{IL} @ V _{IL} = 0.8 V)			10	μA
High Level Output Voltage (V _{OH}) I _{OH} = 4 mA	DVDD - 0.65			V
Low Level Output Voltage (V _{OL}) I _{OL} = 4 mA			0.4	V
Input Capacitance			5	pF

Table 4

Power Supplies

Parameter	Min	Typ	Max	Unit	
Supplies	Voltage, DVDD	3.0	3.3	3.6	V
	Voltage, AVDD	3.0	3.3	3.6	V
Digital Current	Digital Current		56		mA
	Digital Current—Power-Down		2.0		mA
	Analog Current		74		mA
	Analog Current—Power-Down		23		mA
Dissipation	Operation—All Supplies		429		mW
	Operation—Digital Supply		185		mW
	Operation—Analog Supply		244		mW
	Power-Down—All Supplies		83		mW
Power Supply Rejection Ratio	1 kHz 200 mV p-p Signal at Analog Supply Pins		50		dB
	20 kHz 200 mV p-p Signal at Analog Supply Pins		50		dB

Table 5

Temperature Range

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		+70	°C

Table 6

Digital Filters

	Mode	Parameter	Factor	Min	Typ	Max	Unit	
ADC DECIMATION FILTER	All Modes, Typ @ 48 kHz	Pass Band	0.4375 f_s		21		kHz	
		Pass-Band Ripple			±0.015		dB	
		Transition Band	0.5 f_s		24		kHz	
		Stop Band	0.5625 f_s		27		kHz	
		Stop-Band Attenuation		79			dB	
		Group Delay	22.9844/ f_s		479		µs	
DAC INTERPOLATION FILTER	48 kHz Mode, Typ @ 48 kHz	Pass Band	0.4535 f_s		22		kHz	
		Pass-Band Ripple				±0.01	dB	
		Transition Band	0.5 f_s		24		kHz	
		Stop Band	0.5465 f_s		26		kHz	
		Stop-Band Attenuation		70			dB	
		Group Delay	25/ f_s		521		µs	
	96 kHz Mode, Typ @ 96 kHz	Pass Band	0.3646 f_s		35		kHz	
		Pass-Band Ripple					±0.05	dB
		Transition Band	0.5 f_s		48		kHz	
		Stop Band	0.6354 f_s		61		kHz	
		Stop-Band Attenuation		70			dB	
		Group Delay	11/ f_s		115		µs	
	192 kHz Mode, Typ @ 192 kHz	Pass Band	0.3646 f_s		70		kHz	
		Pass-Band Ripple					±0.1	dB
		Transition Band	0.5 f_s		96		kHz	
		Stop Band	0.6354 f_s		122		kHz	
		Stop-Band Attenuation		70			dB	
		Group Delay	8/ f_s		42		µs	

Table 7

Timing Specifications

Parameter		Comments	Min	Max	Unit	
MASTER CLOCK AND RESET	t _{MH}	MCLK High	PLL Mode	20		ns
	t _{ML}	MCLK Low	PLL Mode	20		ns
	t _{MCLK}	MCLK Period	PLL Mode, 256 f_s reference	73	146	ns
	f _{MCLK}	MCLK Frequency	PLL Mode, 256 f_s reference	6.9	13.8	MHz
	t _{MH}	MCLK High	Direct 512 f_s Mode	15		ns
	t _{ML}	MCLK Low	Direct 512 f_s Mode	15		ns
	t _{MCLK}	MCLK Period	Direct 512 f_s Mode	36		ns
	f _{MCLK}	MCLK Frequency	Direct 512 f_s Mode		27.6	MHz
	t _{PDR}	RST Low		15		ns
	t _{PDRR}	RST Recovery	Reset to Active Output	4096		t _{MCLK}
SPI PORT	t _{CCH}	CCLK High		20		ns
	t _{CCL}	CCLK Low		20		ns
	t _{CCP}	CCLK Period		100		ns
	f _{CCLK}	CCLK Frequency			10	MHz
	t _{CDS}	CDATA Setup	To CCLK Rising	10		ns

Parameter		Comments	Min	Max	Unit		
	t _{CDH}	CDATA Hold	From CCLK Rising	10		ns	
	t _{CLS}	CLATCH Setup	To CCLK Rising	10		ns	
	t _{CLH}	CLATCH Hold	From CCLK Falling	10		ns	
	t _{CLH}	CLATCH High		TBD		ns	
	t _{COE}	COUT Enable	From CCLK Falling		20	ns	
	t _{COD}	COUT Delay	From CCLK Falling		25	ns	
	t _{COH}	COUT Hold	From CCLK Falling	20		ns	
	t _{COTS}	COUT Three-State	From CCLK Falling		30	ns	
I ² C PORT		f _{SCL}	SCL Clock Frequency		400	kHz	
		t _{SCLH}	SCL High		0.6	μS	
		t _{SCLL}	SCL Low		1.3	μS	
	Start Condition	t _{SCS}	Setup Time	Relevant for Repeated Start Condition	0.6		μS
		t _{SCH}	Hold Time	After this period the 1st clock is generated	0.6		μS
		t _{DS}	Data Setup Time		100		ns
		t _{SCR}	SCL Rise Time			300	ns
		t _{SCF}	SCL Fall Time			300	ns
		t _{SDR}	SDA Rise Time			300	ns
		t _{SDF}	SDA Fall Time			300	ns
	Stop Condition	t _{SCS}	Setup Time		0.6		μS
DAC SERIAL PORT	Slave Mode	t _{DBH}	DBCLK High		15	ns	
		t _{DBL}	DBCLK Low		15	ns	
		t _{DLS}	DLRCLK Setup	To DBCLK Rising	15		ns
		t _{DLH}	DLRCLK Hold	From DBCLK Rising	15		ns
	Master Mode	t _{DLS}	DLRCLK Skew	From DBCLK Falling	-10	+15	ns
		t _{DDS}	DSDATA Setup	To DBCLK Rising	15		ns
	t _{DDH}	DSDATA Hold	From DBCLK Rising	15		ns	
ADC SERIAL PORT	Slave Mode	t _{ABH}	ABCLK High		15	ns	
		t _{ABL}	ABCLK Low		15	ns	
		t _{ALS}	ALRCLK Setup	To ABCLK Rising	15		ns
		t _{ALH}	ALRCLK Hold	From ABCLK Rising	15		ns
	Master Mode	t _{ALS}	ALRCLK Skew	From ABCLK Falling	-10	+15	ns
		t _{ABDD}	ASDATA Delay	From ABCLK Falling		35	ns
AUXILIARY INTERFACE		t _{AXDS}	AAUXDATA Setup	To AUXBCLK Rising	15		ns
		t _{AXDH}	AAUXDATA Hold	From AUXBCLK Rising	15		ns
		t _{DXDD}	DAUXDATA Delay	From AUXBCLK Falling		35	ns
		t _{XBH}	AUXBCLK High		15		ns
		t _{XBL}	AUXBCLK Low		15		ns
		t _{DLS}	AUXLRCLK Setup	To AUXBCLK Rising	15		ns
		t _{DLH}	AUXLRCLK Hold	From AUXBCLK Rising	15		ns

Table 8

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Analog (AVDD)	-0.3	+3.6	V
Digital (DVDD)	-0.3	+3.6	V
Input Current (Except Supply Pins)		±20	mA
Analog Input Voltage (Signal Pins)	-0.3	AVDD + 0.3	V
Digital Input Voltage (Signal Pins)	-0.3	DVDD + 0.3	V
Ambient Temperature (Operating)	-40	+125	°C
Ambient Temperature (Storage)	-65	+150	°C

Table 9

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Package Characteristics

Parameter	Min	Typ	Max	Unit
θ_{JA} (Thermal Resistance [Junction to Ambient]), 48-lead LQFP		50.1		°C/W
θ_{JC} (Thermal Resistance [Junction to Case]), 48-lead LQFP		17		°C/W
θ_{JA} (Thermal Resistance [Junction to Ambient]), 64-lead LQFP		47		°C/W
θ_{JC} (Thermal Resistance [Junction to Case]), 64-lead LQFP		11.1		°C/W

Note: Characteristics are for a 4-layer board

Table 10



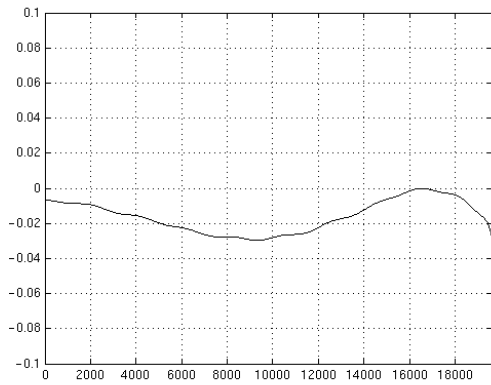


Figure 2. ADC Passband Filter Response, 48 kHz

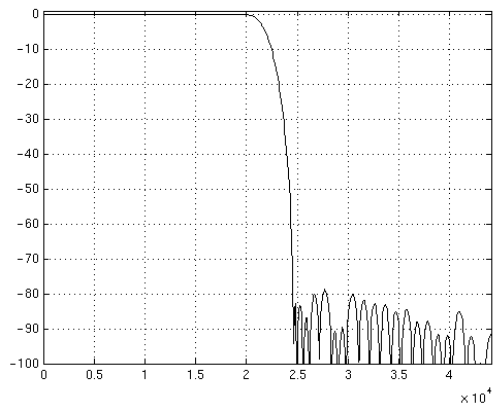


Figure 3. ADC Stopband Filter Response, 48 kHz

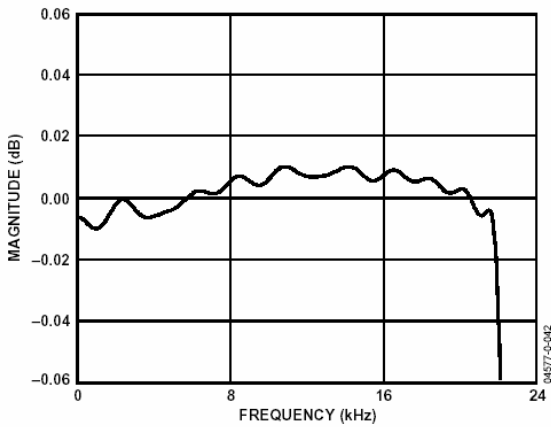


Figure 4. DAC Passband Filter Response, 48 kHz

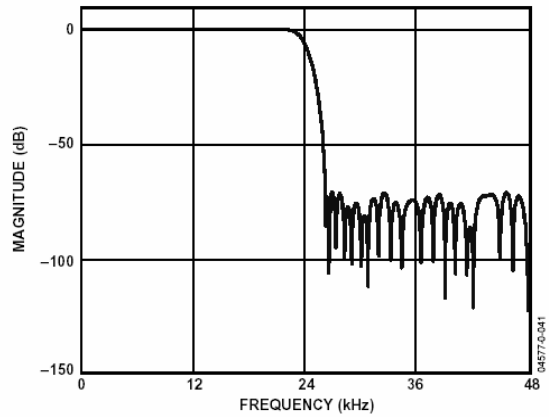


Figure 5. DAC Stopband Filter Response, 48 kHz

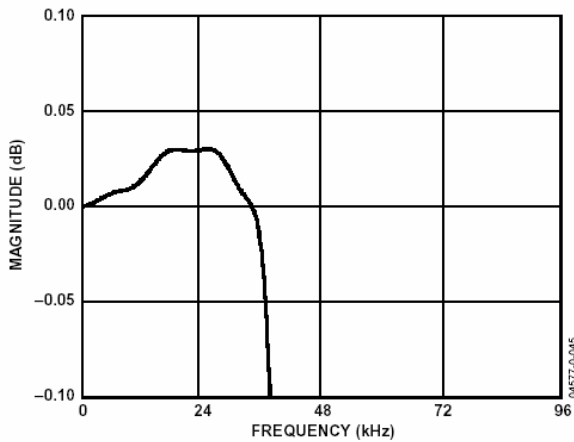


Figure 6. DAC Passband Filter Response, 96 kHz

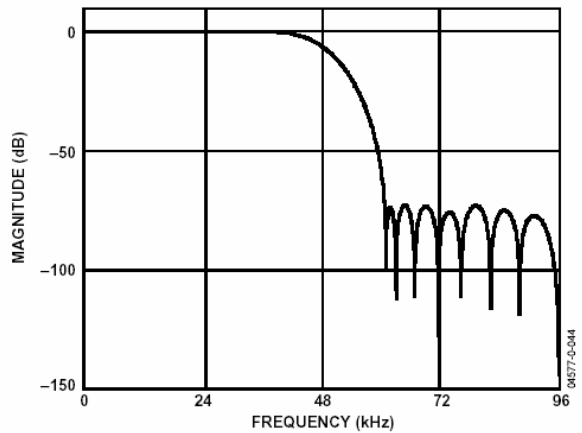


Figure 7. DAC Stopband Filter Response, 96 kHz

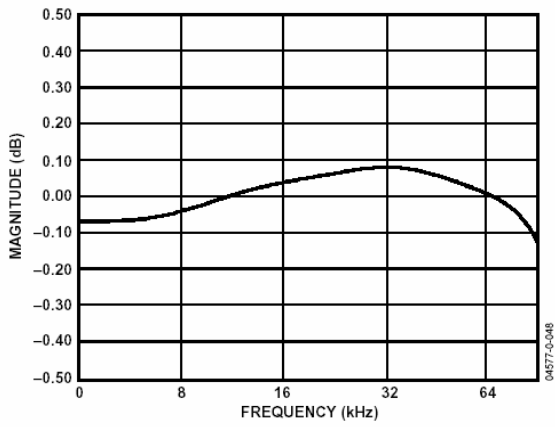


Figure 8. DAC Passband Filter Response, 192 kHz

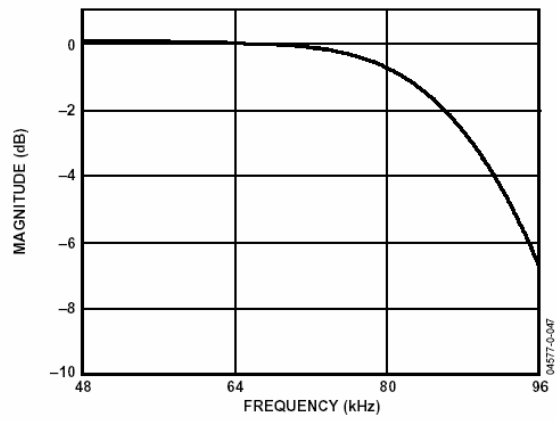


Figure 9. DAC Stopband Filter Response, 192 kHz

FUNCTIONAL OVERVIEW

ADCs

There are two ADC channels in the ADAU132X configured as a stereo pair with differential inputs. The ADCs can operate at a nominal sample rate of 48, 96, or 192 kHz. The ADCs include on-board digital anti-aliasing filters with 79 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 128 (48 kHz, 96 kHz, and 192 kHz modes). Digital output is supplied through a serial data output pin and a frame (ALRCLK) and bit (ABCLK) clock. Alternatively, one of the TDM modes may be used to access up to 16 channels on a single TDM data line.

The ADCs must be driven from a differential signal source for best performance. The input pins of the ADCs connect to internal switched capacitors. To isolate the external driving op amp from the “glitches” caused by the internal switched capacitors, each input pin should be isolated by using a series-connected external 100 Ω resistor together with a 1 nF capacitor connected from each input to ground. This capacitor must be of high quality; for example, ceramic NPO or polypropylene film.

The differential inputs have a nominal common-mode voltage of 1.5V. The voltage at the common-mode reference pin, CM can be used to bias external op amps to buffer the input signals (see the Power Supply and Voltage Reference section). The inputs can also be AC coupled and do not need an external DC bias to CM.

A digital high-pass filter can be switched in line with the ADCs under serial control to remove residual dc offsets. It has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency will scale directly with sample frequency.

DACs

The ADAU132X DAC channels are arranged as four stereo pairs giving eight analog outputs, either single-ended for minimum external components or differential for improved noise and distortion performance. The DACs include on-board digital reconstruction filters with 70 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 4 (48 kHz or 96 kHz modes) or 2 (192 kHz mode). Each channel has its own independently programmable attenuator, adjustable in 255 0.375 dB steps. Digital inputs are supplied through four serial data input pins (one for each stereo pair) and a common frame (DLRCLK) and bit (DBCLK) clock. Alternatively, one of the TDM modes may be used to access up to 16 channels on a single TDM data line.

Each output pin has a nominal common-mode dc level of 1.5V and swings ± 1.27 V for a 0 dBFS digital input signal. A single op amp third order external low-pass filter is recommended to remove high frequency noise present on the output pins, as well as to provide differential-to-single-ended conversion in the case of the differential output part. Note that the use of op amps with low slew rate or low bandwidth may cause high frequency noise and tones to

fold down into the audio band; care should be exercised in selecting these components.

The voltage at the common-mode reference pin, CM can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

Clock Signals

The on-chip Phase Locked Loop (PLL) can be selected to use as its reference the input sample rate from either of the LRCLK pins or 256, 384, 512, or 768 times the sample rate, referenced to 48kHz mode, from the MCLKI pin. The default at power-up is $256 \times f_s$ from MCLKI. In 96 kHz mode, the master clock frequency will stay at the same absolute frequency so the actual multiplication rate will be divided by 2. In 192 kHz mode, the actual multiplication rate will be divided by 4. For example, if the ADAU132X is programmed in $256 \times f_s$ mode, the frequency of the master clock input would be 256×48 kHz = 12.288 MHz. If the ADAU132X is then switched to 96 kHz operation (by writing to the SPI or I²C port), the frequency of the master clock should remain at 12.288 MHz, which is now $128 \times f_s$. In 192kHz mode, this would be $64 \times f_s$.

The internal clock for the ADCs is $256 \times f_s$ for all clock modes. The internal clock for the DACs is $512 \times f_s$ (48 kHz mode), $256 \times f_s$ (96 kHz mode), or $128 \times f_s$ (192 kHz mode). By default, the on-board PLL is used to generate this internal master clock from an external clock. A direct $512 \times f_s$ (referenced to 48 kHz mode) master clock can be used for either the ADCs or DACs if selected in PLL and Clock Control Register 1.

Note that it is not possible to use a direct clock for the ADCs set to 192kHz mode. It is required that the on-chip PLL be used in this mode.

The PLL can be powered down in PLL and Clock Control Register 0. To ensure reliable locking when changing PLL modes or if the reference clock may be unstable at power-on, the PLL should be powered down and then powered back up when the reference clock is stable.

The internal MCLK can be disabled in PLL and Clock Control Register 0 to reduce power dissipation when the ADAU132X is idle. The clock should be stable before it is enabled. Unless a stand-alone mode is selected (see **Serial Control Port**), the clock is disabled by reset and must be enabled by writing to the SPI or I²C port for normal operation.

To maintain the highest performance possible, it is recommended that the clock jitter of the internal master clock signal be limited to less than 300 ps rms TIE (time interval error). Even at these levels, extra noise or tones may appear in the DAC outputs if the jitter spectrum contains large spectral peaks. If the internal PLL is not being used, it is highly recommended that an independent crystal oscillator generate the master clock. In addition, it is especially

important that the clock signal should not be passed through an FPGA, CPLD, or other large digital chip (such as a DSP) before being applied to the ADAU132X. In most cases, this will induce clock jitter due to the sharing of common power and ground connections with other unrelated digital output signals. When the PLL is used, jitter in the reference clock will be attenuated above a certain frequency depending on the loop filter.

Reset and Power-Down

Reset will set all the control registers to their default settings. To avoid pops, reset does not power down the analog outputs. After reset is de-asserted, an initialization routine will run inside the ADAU132X. This initialization lasts for approximately XX MCLKs.

The power-down bits in the PLL and Clock Control 0, DAC Control 1, and ADC Control 1 registers will power down the respective sections. All other register settings are retained.

Serial Control Port

The ADAU132X has an SPI or I²C compatible control port that

permits programming and reading back the internal control registers for the ADCs, DACs, and clock system. There is also a stand-alone mode available for operation without serial control, configured at reset using the serial control pins. All registers are set to default except Internal MCLK Enable is set to 1 and ADC BCLK and LRCLK Master/Slave is set by COUT/SDA. Refer to Table 10 for details.

ADC Clocks:	CIN/ADR0	COUT/SDA	CCLK/SCL	CLATCH/ADR1
Slave	0	0	0	0
Master	0	1	0	0

Table 11. Stand-alone Mode Selection

The SPI control port of the ADAU1328 and ADAU1329 is a 4-wire serial control port. The format is similar to the Motorola SPI format except the input data-word is 24 bits wide. The serial bit clock and latch may be completely asynchronous to the sample rate of the ADCs and DACs. Figure 10 shows the format of the SPI signal. The first byte is a global address with a read/write bit. For the ADAU132X the address is 0x04, shifted left 1 bit due to the R/W bit. The second byte is the ADAU132X register address and the third byte is the data.

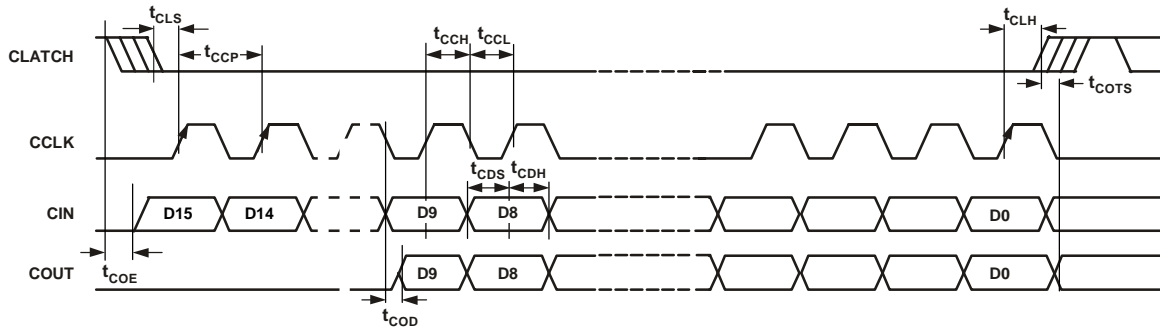


Figure 10. Format of SPI Signal

The I²C interface of the ADAU1326 and ADAU1327 is a two wire interface consisting of a clock line, SCL and a data line, SDA. SDA is bidirectional and the ADAU1326 and ADAU1327 will drive SDA either to acknowledge the master, ACK, or to send data during a read operation. The SDA pin for the I²C port is an open drain collector and requires a 1KΩ pullup resistor. A write or read access occurs when the SDA line is pulled low while the SCL line is high indicated by START in the timing diagrams. SDA is only allowed to change when SCL is low except when a START or STOP condition occurs as shown in figures 3 and 4. The first eight bits of the access consist of the device address and the R/W bit. The device address consists of an internal built-in address (0x04) and two address pins, AD1 and AD0. The two address pins allow up to four ADAU1326s and ADAU1327s to be used in a system. Initiating a write operation to the ADAU1326 and ADAU1327 involves sending a START condition and then sending the device address with the R/W set low. The ADAU1326 and ADAU1327 will respond by issuing an ACK to indicate that it has been addressed. The user then sends a second frame telling the ADAU1326 and ADAU1327 which register

is required to be written to. Another ACK is issued by the ADAU1326 and ADAU1327. Finally the user can send another frame with the 8 data bits required to be written to the register. A third ACK is issued by the ADAU1326 and ADAU1327 after which the user can send a STOP condition to complete the data transfer.

A read operation requires that the user first write to the ADAU1326 and ADAU1327 to point to the correct register and then read the data. This is achieved by sending a START condition followed by the device address frame, with R/W low, and then the register address frame. Following the ACK from the ADAU1326 and ADAU1327 the user must issue a REPEATED START condition. This is identical to a START condition. The next frame is the device address with R/W set high. On the next frame the ADAU1326 and ADAU1327 will output the register data on the SDA line. A STOP condition completes the read operation. Figure 3 and Figure 4 show examples of writing to and reading from the DAC 1 Left Volume Register (address = 0x06)

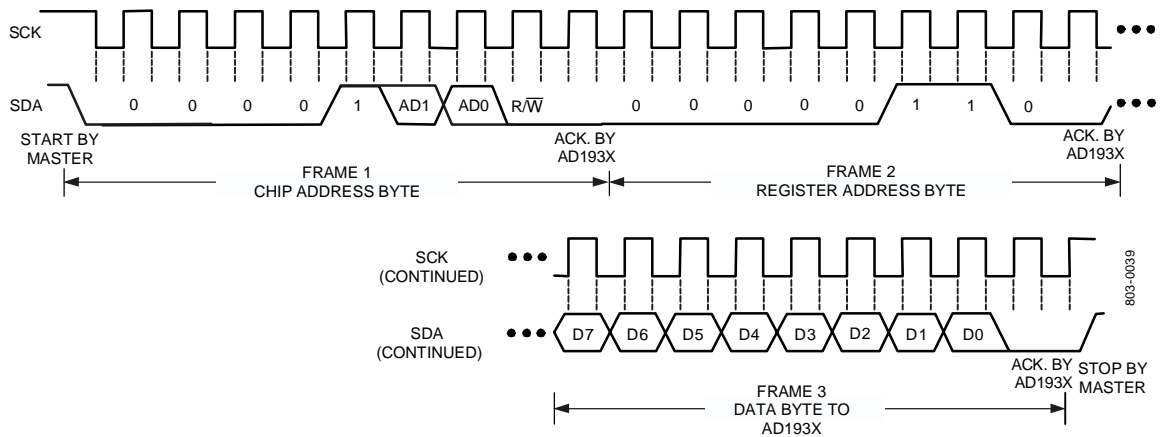


Figure 11. Format of I²C Write

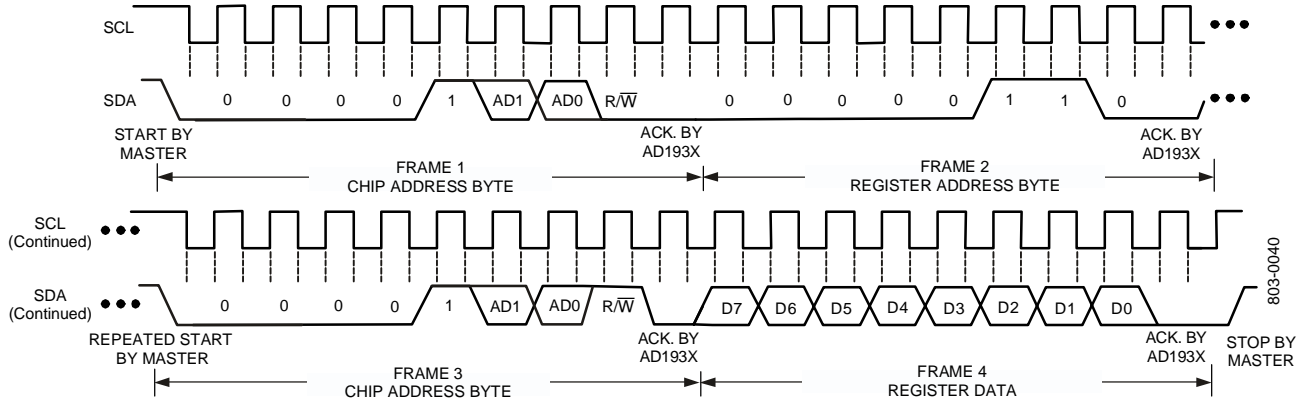


Figure 12. Format of I²C Read

Power Supply and Voltage Reference

The ADAU132X is designed for 3.3 V supplies. Separate power supply pins are provided for the analog and digital sections. These pins should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 22 μF should also be provided on the same PC board as the codec. For critical applications, improved performance will be obtained with separate supplies for the analog and digital sections. If this is not possible, it is recommended that the analog and digital supplies be isolated by means of a ferrite bead in series with each supply. It is important that the analog supply be as clean as possible.

The AD1935 (64-pin single-ended version), and the ADAU1329 and ADAU1327 (64-pin differential versions) include a 3.3V regulator driver which requires only an external pass transistor and bypass capacitors to make a 5V to 3.3V regulator. If the regulator driver is not used, VSUPPLY, VDRIVE, and VSENSE should be connected to DGND.

All digital inputs are compatible with TTL and CMOS levels. All

outputs are driven from the 3.3 V DVDD supply and are compatible with TTL and 3.3 V CMOS levels.

The ADC and DAC internal voltage reference V_{REF} is brought out on FILTR and should be bypassed as close as possible to the chip, with a parallel combination of 10 μF and 100 nF. Any external current drawn should be limited to less than 50 μA.

The internal reference can be disabled in PLL and Clock Control Register 1 and FILTR driven from an external source. This can be used to scale the DAC output to a power amplifier's clipping level based on its power supply voltage. The ADC input gain will also vary by the inverse ratio. The total gain from ADC input to DAC output will stay constant.

The CM pin is the internal common-mode reference. It should be bypassed as close as possible to the chip, with a parallel combination of 47 μF and 100 nF. This voltage may be used to bias external op amps to the common-mode voltage of the input and output signal pins. The output current should be limited to less than 0.5 mA source and 2 mA sink.

Serial Data Ports—Data Format

The eight DAC channels output or accept a common serial bit clock and left-right framing clock to clock in the serial data. The two ADC channels output or accept a serial bit clock and left-right framing clock to clock out the data. The clock signals are all synchronous with the sample rate. In the AUX Modes, set in ADC Control 1 and DAC Control 0, the DACs use the ADC serial bit clock and left-right clock as the DAC clock pins are used for the auxiliary ADC/DAC serial clocks.

The ADC and DAC serial data modes default to I²S. The ports can also be programmed for left-justified, right-justified and TDM modes. The word width is 24 bits by default and can be programmed for 16 or 20 bits. The normal TDM mode can be

daisy-chained with a second ADAU132X and will support 16 channels at 48 kHz, 8 channels at 96 kHz or 4 channels at 192 kHz. There is also a dual-line TDM mode to support 8 channels at 192 kHz.

The special auxiliary modes are provided to allow two external stereo ADCs and/or two external stereo DACs to be interfaced with the ADAU132X to provide up to 6 in/12 out operation or 2 ADAU132Xs to be chained for up to 12 in/16 out operation. These modes provide a glueless interface to a single SHARC serial port, allowing the DSP to access up to 16 channels of analog I/O. In these modes many pins are redefined, see table 10. See Figure 18 for details of these modes.

The following figures show the serial mode formats.

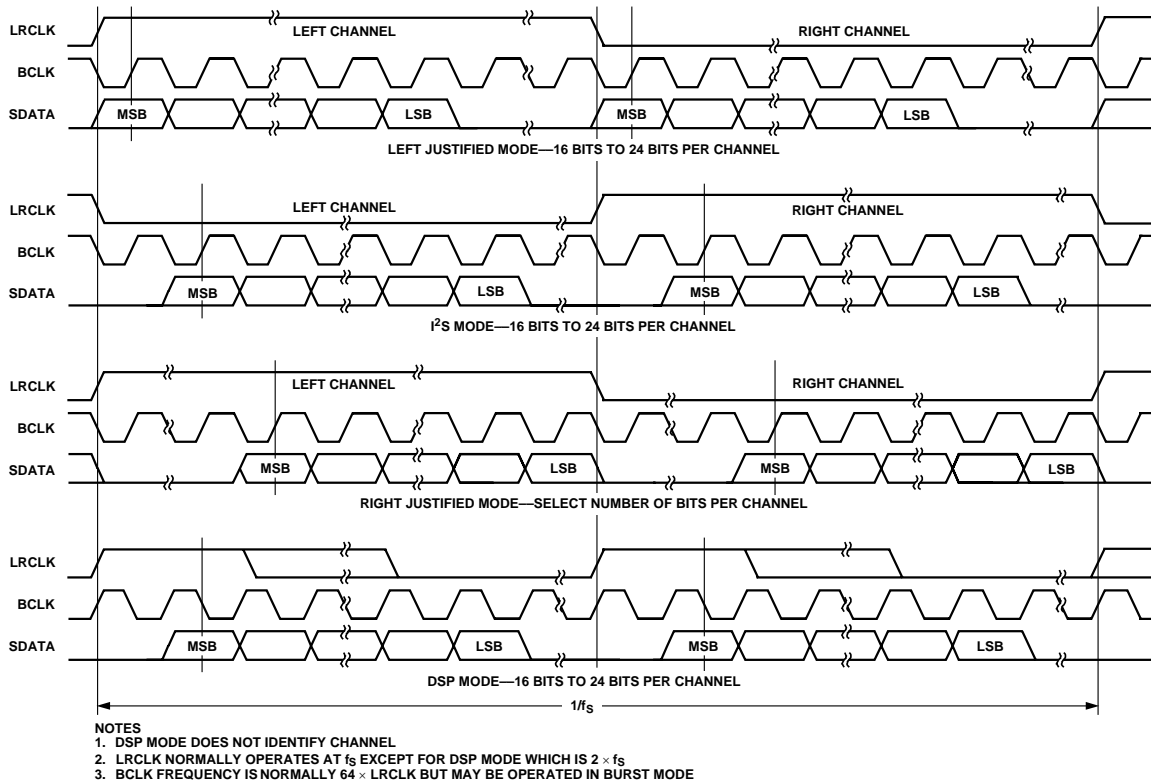


Figure 13. Stereo Serial Modes

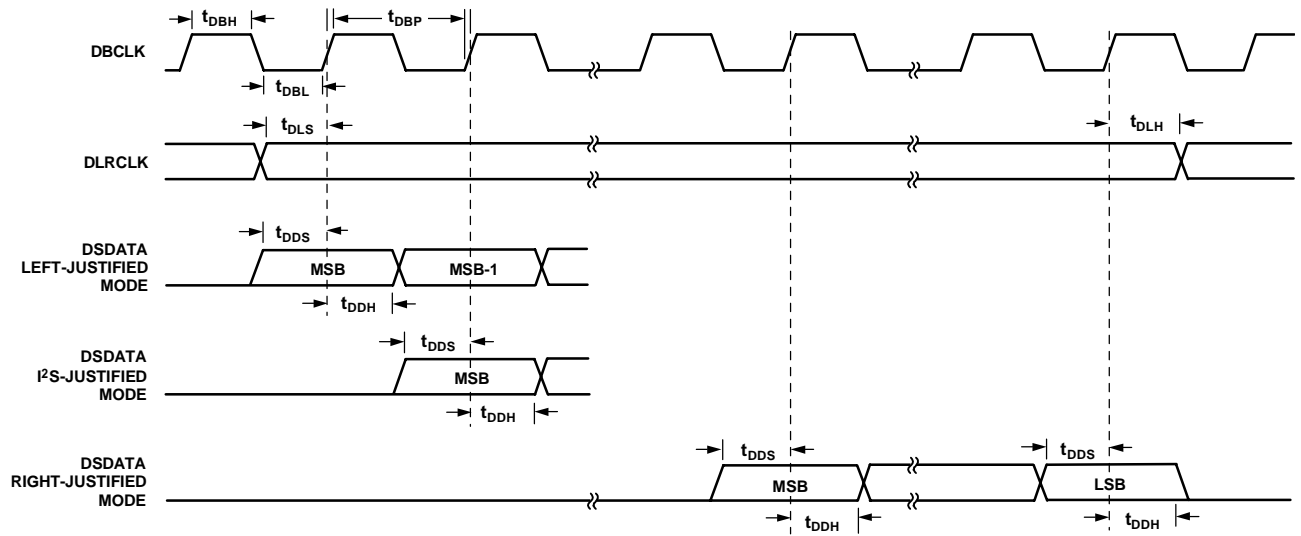


Figure 14. DAC Serial Timing

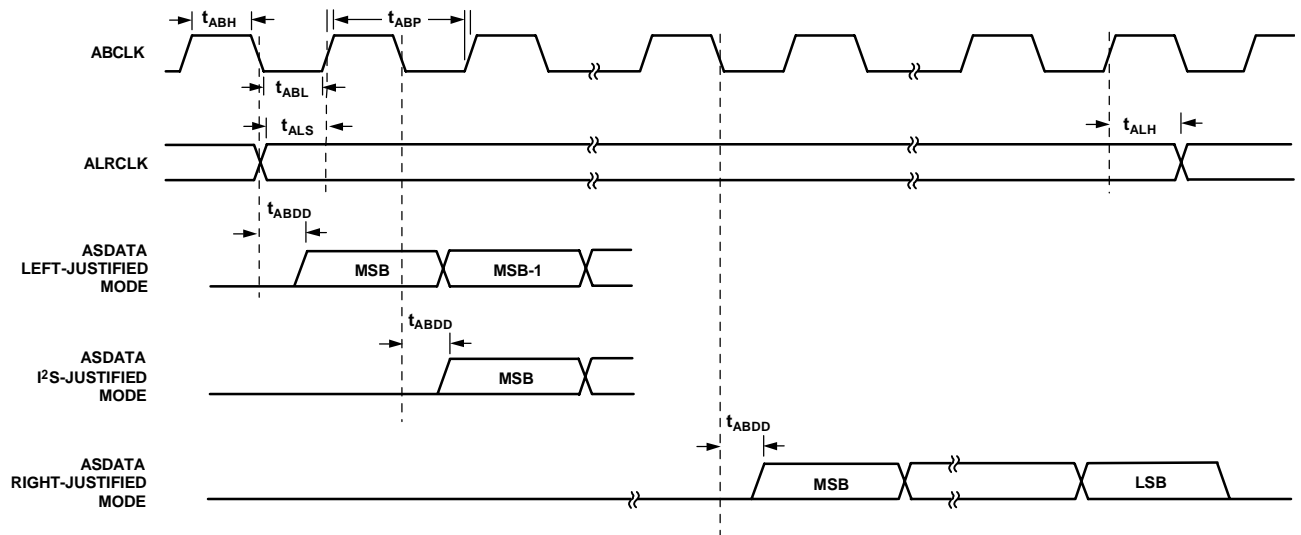


Figure 15. ADC Serial Timing

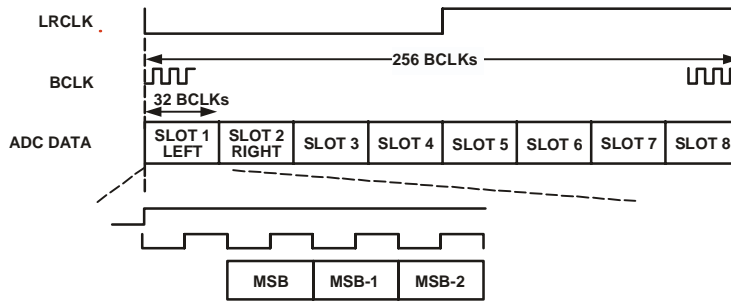


Figure 16. ADC TDM (8-channel I²S mode)

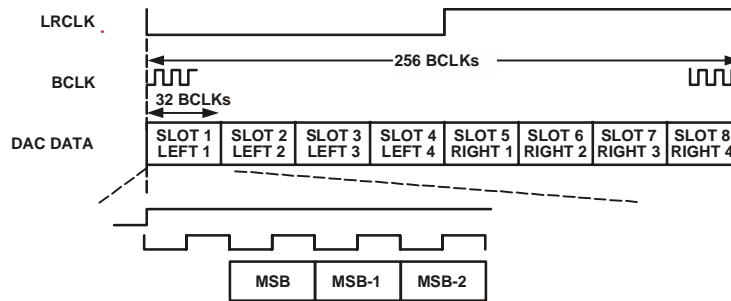
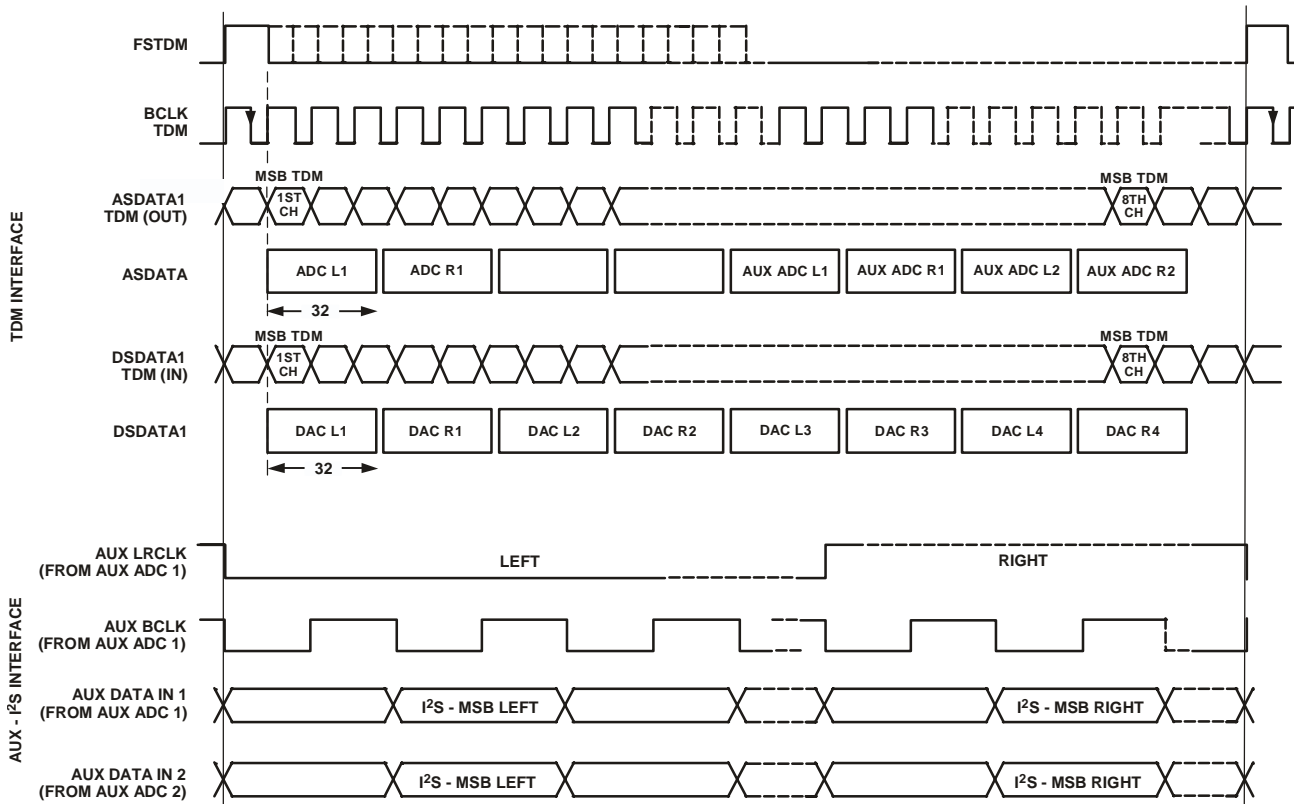


Figure 17. DAC TDM (8-channel I²S mode)



AUX BCLK FREQUENCY IS 64 × FRAME-RATE; TDM BCLK FREQUENCY IS 256 × FRAME-RATE.

Figure 18. AUX 256 Mode Timing (Note that the Clocks Are Not to Scale)

Pin Function Changes in TDM and AUX Modes

Pin Name	Stereo Modes	TDM Modes	AUX Modes
ASDATA1	ADC Data Out	ADC TDM Data Out	TDM Data Out
ASDATA2		ADC TDM Data In	AUX Data Out 1 (to Ext. DAC 1)
DSDATA1	DAC1 Data In	DAC TDM Data In	TDM Data In
DSDATA2	DAC2 Data In	DAC TDM Data Out	AUX Data In 1 (from Ext. ADC 1)
DSDATA3	DAC3 Data In	DAC TDM Data In 2 (dual-line mode)	AUX Data In 2 (from Ext. ADC 2)
DSDATA4	DAC4 Data In	DAC TDM Data Out 2 (dual-line mode)	AUX Data Out 2 (to Ext. DAC 2)
ALRCLK	ADC LRCLK In/Out	ADC TDM Frame Sync In/Out	TDM Frame Sync In/Out
ABCLK	ADC BCLK In/Out	ADC TDM BCLK In/Out	TDM BCLK In/Out
DLRCLK	DAC LRCLK In/Out	DAC TDM Frame Sync In/Out	AUX LRCLK In/Out
DBCLK	DAC BCLK In/Out	DAC TDM BCLK In/Out	AUX BCLK In/Out

Table 12

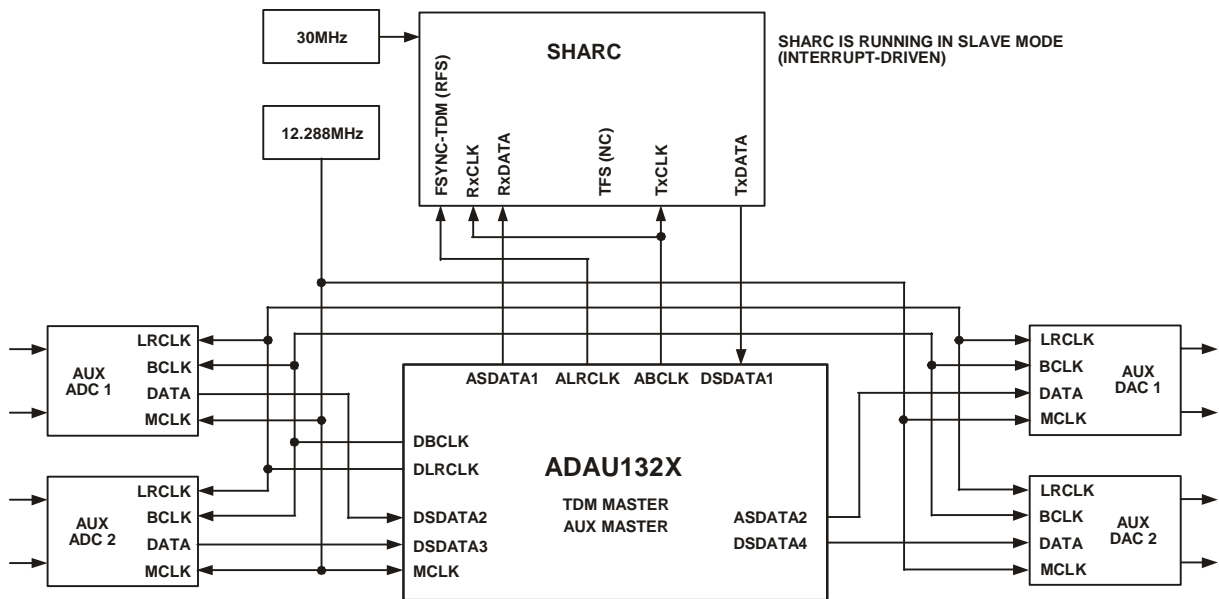


Figure 19. Example of AUX Mode Connection to SHARC (ADAU132X as TDM Master/AUX Master shown)

PIN FUNCTION DESCRIPTIONS

48-Lead LQFP Plastic Package – ADAU1326, ADAU1328

Pin No.	In/Out	Mnemonic	Description
1	I	AGND	Analog Ground.
2	I	MCLKI/XI	Master Clock Input/ Crystal Oscillator Input.
3	O	MCLK/XO	Master Clock Output/ Crystal Oscillator Output.
4	I	AGND	Analog Ground.
5	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
6	O	OL3	DAC 3 Left Output.
7	O	OR3	DAC 3 Right Output.
8	O	OL4	DAC 4 Left Output.
9	O	OR4	DAC 4 Right Output.
10	I	RST	Reset (Active Low).
11	I/O	DSDATA4	DAC Input 4 (Input to DAC 4 L and R)/DAC TDM Data Out 2/AUX ADC 1 Data In.
12	I	DGND	Digital Ground.
13	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
14	I/O	DSDATA3	DAC Input 3 (Input to DAC 3 L and R)/DAC TDM Data In 2/Aux DAC 2 Data Output.
15	I/O	DSDATA2	DAC Input 2 (Input to DAC 2 L and R)/DAC TDM Data Out/AUX ADC 1 Data In.
16	I	DSDATA1	DAC Input 1 (Input to DAC 1 L and R)/DAC TDM Data In/AUX ADC 2 Data In.
17	I/O	DBCLK	Bit Clock for DACs.
18	I/O	DLRCLK	LR Clock for DACs.
19	I/O	ASDATA2	ADC TDM Data Input/Aux DAC 1 Data Output.
20	O	ASDATA1	ADC Serial Data Output (ADC L and R)/ADC TDM Data Output.
21	I/O	ABCLK	Bit Clock for ADCs.
22	I/O	ALRCLK	LR Clock for ADCs.
23	O	CIN/ADR0	Control Data Input (SPI)/Address 0 (I ² C).
24	I	COUT/SDA	Control Data Output (SPI)/Serial Data (I ² C).
25	I	DGND	Digital Ground.
26	I	CCLK/SCL	Control Clock Input (SPI)/Serial Clock (I ² C).
27	I	CLATCH/ADR1	Latch Input for Control Data (SPI)/Address 1 (I ² C).
28	O	OL1	DAC 1 Left Output.
29	O	OR1	DAC 1 Right Output.
30	O	OL2	DAC 2 Left Output.
31	O	OR2	DAC 2 Right Output.
32	I	AGND	Analog Ground.
33	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
34	I	AGND	Analog Ground.
35	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass with 10 μ F 100 nF to AGND.
36	I	AGND	Analog Ground.
37	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
38	O	CM	Common Mode Reference Filter Capacitor Connection. Bypass with 47 μ F 100 nF to AGND.
39	I	ADC1LP	ADC1 Left Positive Input.
40	I	ADC1LN	ADC1 Left Negative Input.
41	I	ADC1RP	ADC1 Right Positive Input.
42	I	ADC1RN	ADC1 Right Negative Input.
43			No Connect.
44			No Connect.
45			No Connect.
46			No Connect.
47	O	LF	PLL Loop Filter, Return to AVDD.
48	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.

Table 13. Pin Function Description—48-Lead LQFP(ADAU1326, ADAU1328)

64-Lead LQFP Plastic Package – ADAU1327, ADAU1329

Pin No.	In/Out	Mnemonic	Description
1	I	AGND	Analog Ground.
2	I	MCLKI/XI	Master Clock Input/ Crystal Oscillator Input.
3	O	MCLK/XO	Master Clock Output/ Crystal Oscillator Output.
4	I	AGND	Analog Ground.
5	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
6	O	OL3P	DAC 3 Left Positive Output.
7	O	OL3N	DAC 3 Left Negative Output.
8	O	OR3P	DAC 3 Right Positive Output.
9	O	OR3N	DAC 3 Right Negative Output.
10	O	OL4P	DAC 4 Left Positive Output.
11	O	OL4N	DAC 4 Left Negative Output.
12	O	OR4P	DAC 4 Right Positive Output.
13	O	OR4N	DAC 4 Right Negative Output.
14	I	RST	Reset (Active Low).
15	I/O	DSDATA4	DAC Input 4 (Input to DAC 4 L and R)/DAC TDM Data Out 2/AUX ADC 1 Data In.
16	I	DGND	Digital Ground.
17	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
18	I/O	DSDATA3	DAC Input 3 (Input to DAC 3 L and R)/DAC TDM Data In 2/Aux DAC 2 Data Output.
19	I/O	DSDATA2	DAC Input 2 (Input to DAC 2 L and R)/DAC TDM Data Out/AUX ADC 1 Data In.
20	I	DSDATA1	DAC Input 1 (Input to DAC 1 L and R)/DAC TDM Data In/AUX ADC 2 Data In.
21	I/O	DBCLK	Bit Clock for DACs.
22	I/O	DLRCLK	LR Clock for DACs.
23	I	VSUPPLY	+5V Input to Regulator, Emitter of Pass Transistor
24	I	VSENSE	+3.3V Output of Regulator, Collector of Pass Transistor
25	O	VDRIVE	Drive for Base of Pass Transistor
26	I/O	ASDATA2	ADC TDM Data Input/Aux DAC 1 Data Output.
27	O	ASDATA1	ADC Serial Data Output (ADC L and R)/ADC TDM Data Output.
28	I/O	ABCLK	Bit Clock for ADCs.
29	I/O	ALRCLK	LR Clock for ADCs.
30	I	CIN/ADR0	Control Data Input (SPI)/Address 0 (I ² C).
31	I/O	COUT/SDA	Control Data Output (SPI)/Serial Data (I ² C).
32	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
33	I	DGND	Digital Ground.
34	I	CCLK/SCL	Control Clock Input (SPI)/Serial Clock (I ² C).
35	I	CLATCH/ADR1	Latch Input for Control Data (SPI)/Address 1 (I ² C).
36	O	OL1P	DAC 1 Left Positive Output.
37	O	OL1N	DAC 1 Left Negative Output.
38	O	OR1P	DAC 1 Right Positive Output.
39	O	OR1N	DAC 1 Right Negative Output.
40	O	OL2P	DAC 2 Left Positive Output.
41	O	OL2N	DAC 2 Left Negative Output.
42	O	OR2P	DAC 2 Right Positive Output.
43	O	OR2N	DAC 2 Right Negative Output.
44	I	AGND	Analog Ground.
45	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
46	I	AGND	Analog Ground.
47	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass with 10 μ F 100 nF to AGND.
48	I	AGND	Analog Ground.
49			No Connect.
50			No Connect.
51	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.

Pin No.	In/Out	Mnemonic	Description
52	O	CM	Common Mode Reference Filter Capacitor Connection. Bypass with 47 μ F 100 nF to AGND.
53	I	ADC1LP	ADC1 Left Positive Input.
54	I	ADC1LN	ADC1 Left Negative Input.
55	I	ADC1RP	ADC1 Right Positive Input.
56	I	ADC1RN	ADC1 Right Negative Input.
57			No Connect.
58			No Connect.
59			No Connect.
60			No Connect.
61	O	LF	PLL Loop Filter, Return to AVDD.
62	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
63			No Connect.
64			No Connect.

Table 14. Pin Function Description—64-Lead LQFP (ADAU1327, ADAU1329)

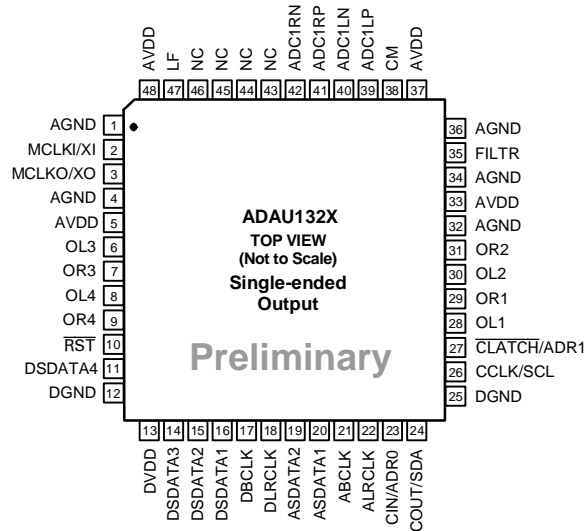
PIN CONFIGURATION


Figure 20. Single-ended Output 48-Lead LQFP (ADAU1326, ADAU1328)

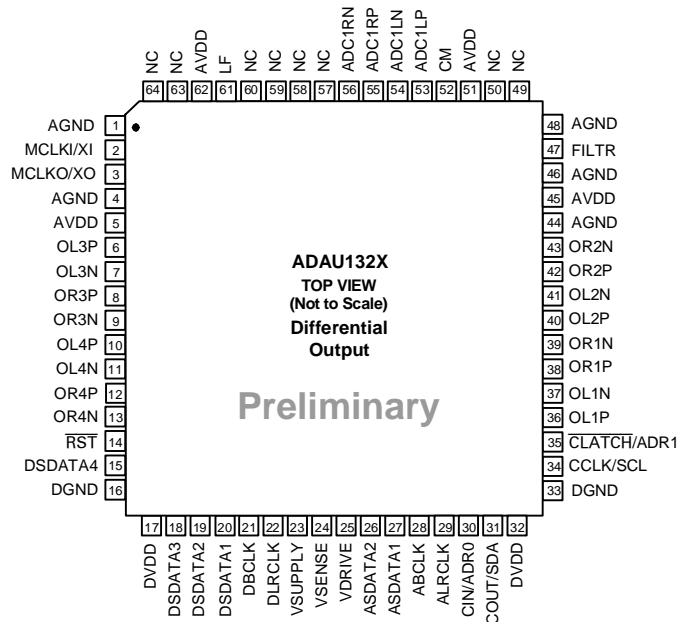


Figure 21. Differential Output 64-Lead LQFP (ADAU1327, ADAU1329)

APPLICATION CIRCUITS

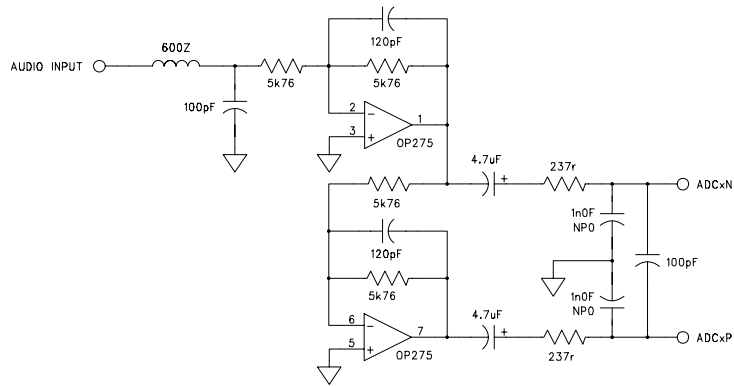


Figure 22. Typical ADC Input Filter Circuit

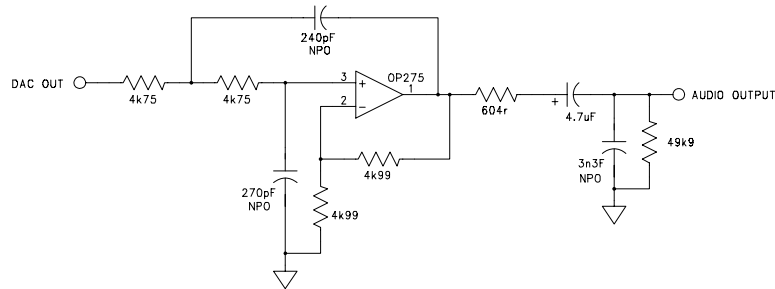


Figure 23. Typical DAC Output Filter Circuit (Single-ended, Non-inverting)

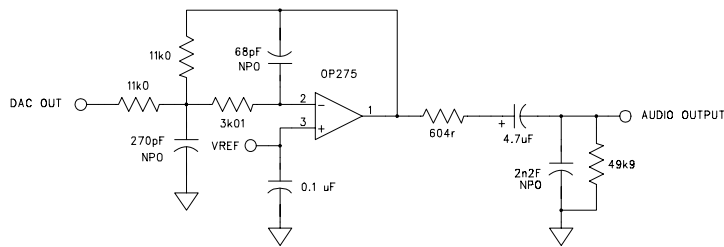


Figure 24. Typical DAC Output Filter Circuit (Single-ended, Inverting)

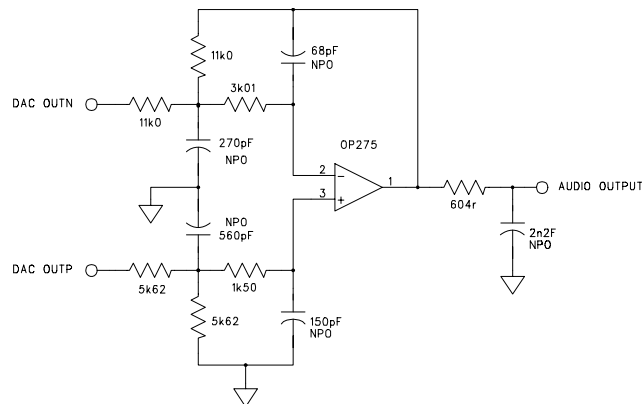


Figure 25. Typical DAC Output Filter Circuit (Differential)

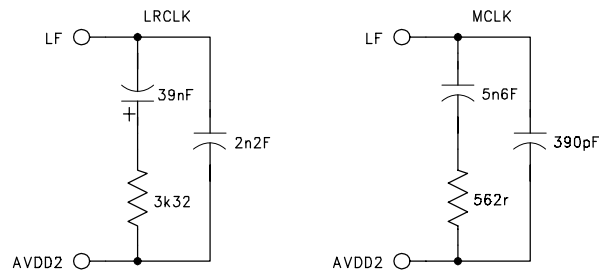


Figure 26. Recommended Loop Filters for LRCLK or MCLK PLL reference.

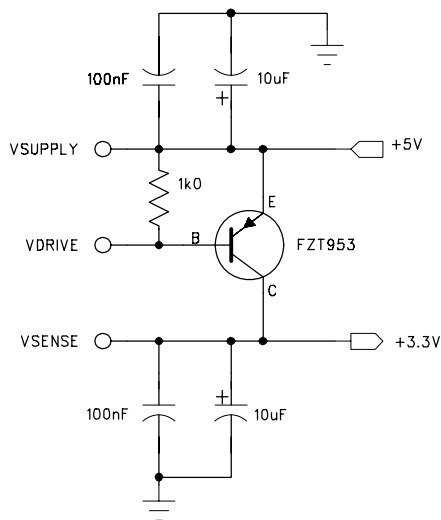


Figure 27. Recommended 3.3V Regulator Circuit (64-lead versions)

REGISTER DEFINITIONS

Register format

	Global Address	R/W	Register Address	Data
Bit	23:17	16	15:8	7:0

Table 15

Note 1: The format is the same for I²C and SPI.

Note 2: Global address for the ADAU132X series is 0x04, shifted left 1 bit due to the R/W bit.

Note 3: In I²C, ADR0 and ADR1 are ORed into bits 17 and 18 to provide multiple chip addressing.

Note 4: All registers are reset to 0, except for the DAC volume registers which are set to full volume.

Register addresses and functions

Address	Function
0	PLL and Clock Control 0
1	PLL and Clock Control 1
2	DAC Control 0
3	DAC Control 1
4	DAC Control 2
5	DAC Individual Channel Mutes
6	DAC 1L Vol Control
7	DAC 1R Vol Control
8	DAC 2L Vol Control
9	DAC 2R Vol Control
10	DAC 3L Vol Control
11	DAC 3R Vol Control
12	DAC 4L Vol Control
13	DAC 4R Vol Control
14	ADC Control 0
15	ADC Control 1
16	ADC Control 2

Table 16

PLL AND CLOCK CONTROL REGISTERS**PLL and Clock control 0**

Bit	Value	Function	Description
0	0	Normal operation	PLL power down
	1	Power down	
2:1	00	INPUT 256 (x 44.1 or 48kHz)	MCLK pin functionality (PLL active)
	01	INPUT 384 (x 44.1 or 48kHz)	
	10	INPUT 512 (x 44.1 or 48kHz)	
	11	INPUT 768 (x 44.1 or 48kHz)	
4:3	00	XTAL Oscillator Enabled	MCLK_O pin
	01	256xfs VCO Output	
	10	512xfs VCO Output	
	11	Off	
6:5	00	MCLK	PLL input
	01	DLRCLK	
	10	ALRCLK	
	11	Reserved	
7	0	Disable: ADC and DAC Idle	Internal MCLK Enable
	1	Enable: ADC and DAC Active	

Table 17

PLL and Clock control 1

Bit	Value	Function	Description
0	0	PLL Clock	DAC Clock Source Select
	1	MCLK	
1	0	PLL Clock	ADC Clock Source Select
	1	MCLK	
2	0	Enabled	On-chip Voltage Reference
	1	Disabled	
3	0	Not Locked	PLL Lock Indicator (Read Only)
	1	Locked	
7:4	0000	Reserved	

Table 18

DAC CONTROL REGISTERS

DAC control 0

Bit	Value	Function	Description
0	0	Normal	Power Down
	1	Power down	
2:1	00	32/44.1/48 kHz	Sample Rate
	01	64/88.2/96 kHz	
	10	128/176.4/192 kHz	
	11	Reserved	
5:3	000	1	SDATA Delay (BCLK periods)
	001	0	
	010	8	
	011	12	
	100	16	
	101	Reserved	
	110	Reserved	
	111	Reserved	
7:6	00	Stereo (Normal)	Serial Format
	01	TDM (Daisy Chain)	
	10	DAC Aux mode (ADC, DAC TDM coupled)	
	11	Dual-line TDM	

Table 19

DAC control 1

Bit	Value	Function	Description
0	0	Latch in mid cycle (normal)	BCLK Active Edge (TDM In)
	1	Latch in at end of cycle (pipeline)	
2:1	00	64 (2 channels)	BCLKs Per Frame
	01	128 (4 channels)	
	10	256 (8 channels)	
	11	512 (16 channels)	
3	0	Left low	LRCLK Polarity
	1	Left high	
4	0	Slave	LRCLK Master/Slave
	1	Master	
5	0	Slave	BCLK Master/Slave
	1	Master	
6	0	DBCLK pin	BCLK Source
	1	Internally generated	
7	0	Normal	BCLK Polarity
	1	Inverted	

Table 20

DAC control 2

Bit	Value	Function	Description
0	0	Unmute	Master Mute
	1	Mute	
2:1	00	Flat	Deemphasis (32/44.1/48 kHz mode only)
	01	48 kHz Curve	
	10	44.1 kHz Curve	
	11	32 kHz Curve	
4:3	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
5	0	Non-inverted	DAC Output Polarity
	1	Inverted	
7:6	00	Reserved	

Table 21

DAC Individual Channel Mutes

Bit	Value	Function	Description
0	0	Unmute	DAC 1 Left Mute
	1	Mute	
1	0	Unmute	DAC 1 Right Mute
	1	Mute	
2	0	Unmute	DAC 2 Left Mute
	1	Mute	
3	0	Unmute	DAC 2 Right Mute
	1	Mute	
4	0	Unmute	DAC 3 Left Mute
	1	Mute	
5	0	Unmute	DAC 3 Right Mute
	1	Mute	
6	0	Unmute	DAC 4 Left Mute
	1	Mute	
7	0	Unmute	DAC 4 Right Mute
	1	Mute	

Table 22

DAC Volume Controls

Bit	Value	Function	Description
7:0	0	No attenuation	DAC Volume Control
	1-254	-3/8 dB per step	
	255	Full Attenuation	

Table 23

ADC CONTROL REGISTERS

ADC control 0

Bit	Value	Function	Description
0	0	Normal	Power Down
	1	Power down	
1	0	Off	Highpass Filter
	1	On	
2	0	Unmute	ADC 1L mute
	1	Mute	
3	0	Unmute	ADC 1R mute
	1	Mute	
4	0	Reserved	
5	0	Reserved	
7:6	00	32/44.1/48	Output Sample Rate
	01	64/88.2/96	
	10	128/176.4/192	
	11	Reserved	

Table 24

ADC control 1

Bit	Value	Function	Description
1:0	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
4:2	000	1	SDATA delay (BCLK periods)
	001	0	
	010	8	
	011	12	
	100	16	
	101	Reserved	
	110	Reserved	
	111	Reserved	
6:5	00	Stereo	Serial Format
	01	TDM (Daisy Chain)	
	10	ADC Aux mode (ADC, DAC TDM coupled)	
	11	Reserved	
7	0	Latch in mid cycle (normal)	BCLK Active Edge (TDM In)
	1	Latch in at end of cycle (pipeline)	

Table 25.

ADC control 2

Bit	Value	Function	Description
0	0	50/50 (allows 32/24/20/16 BCLK/channel)	LRCLK Format
	1	Pulse (32 BCLK/channel)	
1	0	Drive out on falling edge (DEF)	BCLK Polarity
	1	Drive out on rising edge	
2	0	Left Low	LRCLK Polarity
	1	Left High	
3	0	Slave	LRCLK Master/Slave
	1	Master	
5:4	00	64	BCLKs per frame
	01	128	
	10	256	
	11	512	
6	0	Slave	BCLK Master/Slave
	1	Master	
7	0	ABCLK pin	BCLK Source
	1	Internally generated	

Table 26

OUTLINE DIMENSIONS

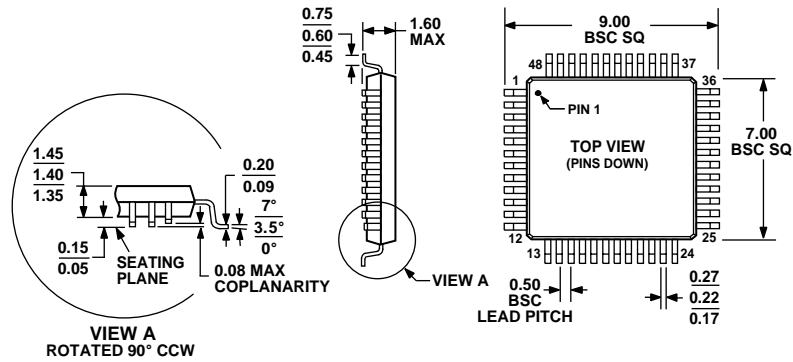


Figure 28. 48-Lead Low Profile Quad Flat Package [LQFP] (ST-48)
Dimensions shown in millimeters

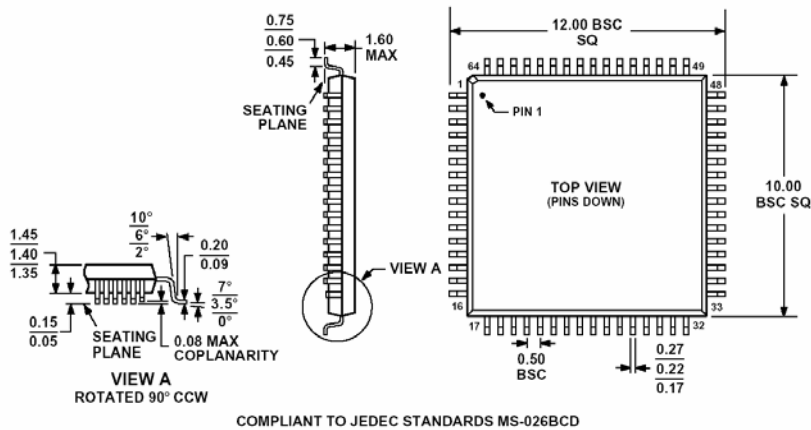


Figure 29. 64-Lead Low Profile Quad Flat Package [LQFP] (ST-64)
Dimensions shown in millimeters

Ordering Guide

ADAU132X Products	Temperature Package (ambient)	Package Description	Package Option
ADAU1326XSTZ	0°C to +70°C	48-Lead LQFP, SE out, I ² C control	ST-48
ADAU1326XSTZRL	0°C to +70°C	48-Lead LQFP, SE out, I ² C control	ST-48 on 13" Reels
ADAU1327XSTZ	0°C to +70°C	64-Lead LQFP, Diff out, I ² C control	ST-64
ADAU1327XSTZRL	0°C to +70°C	64-Lead LQFP, Diff out, I ² C control	ST-64 on 13" Reels
ADAU1328XSTZ	0°C to +70°C	48-Lead LQFP, SE out, SPI control	ST-48
ADAU1328XSTZRL	0°C to +70°C	48-Lead LQFP, SE out, SPI control	ST-48 on 13" Reels
ADAU1329XSTZ	0°C to +70°C	64-Lead LQFP, Diff out, SPI control	ST-64
ADAU1329XSTZRL	0°C to +70°C	64-Lead LQFP, Diff out, SPI control	ST-64 on 13" Reels
EVAL-ADAU1326EB		ADAU1326 Evaluation Board	
EVAL-ADAU1327EB		ADAU1327 Evaluation Board	
EVAL-ADAU1328EB		ADAU1328 Evaluation Board	
EVAL-ADAU1329EB		ADAU1329 Evaluation Board	

Note: All parts are lead-free

Table 27. Ordering Guide

Notes