DP2

User Manual

Revision 0.2
25th April 2008

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Introduction

DP2 is an Altera FPGA development board, aimed principally at the development of low cost audio and video products.
The heart of the board is an Altera EP2C8 FPGA which offers an excellent compromise between resources and cost. The FPGA offers 8256 logic elements, 165,888 bits of RAM organized as 36 M4K RAM blocks, 36 18x18 multipliers and 2 PLLs. The package used is the 144 pin TQFP, again offering a good compromise between cost and I/O count; 85 I/O pins are available to the user.
Most of the I/O of the board is taken out to two expansion connectors. The first of these is designed to accept the SingMai DP1 card which provides audio and video ADC and DAC functionality. The second can be used for additional I/O interfaces or for a FIFO memory such as the SingMai DP3.
In addition the card provides some control interfaces such as five push button switches, two hexadecimal displays and an optical encoder. The board also offers a connector compatible with the Optrex range of character LCD displays, and also a USB interface via the DLP-245 USB adapter. Optical audio interfaces are also provided, one transmitter and one receiver.
There are on-board linear power supplies to optimize the signal to noise ratio of the ADCs and DACs; the board requires a single 9V DC input.

Unpacking DP2

The DP2 should arrive without obvious damage to the box. Inside the box you should find the DP2 board and a CD which contains the user manual, datasheets, circuit diagrams and other associated files. The DP2 board is supplied in an anti-static bag and when removed from the bag normal anti-static precautions should be observed, (e.g. hold the board by the edges). If there are any signs of damage to the board or CD please contact SingMai Electronics at enquiries@singmai.com.

What is on the CD?

Place the CD into your drive and you should be prompted with what action to take: choose open folder to show files and folders. If you are not prompted automatically, use windows explorer to point to your CD drive (usually D: or E:). You should see various folders on the drive, Datasheets, FPGA designs, Schematics and User Manual. Each folder contains,

- **Datasheets**: Contains the detailed datasheets for each of the ICs used on the DP2 board.
- **FPGA designs**: Contains example FPGA design files for the DP2 with examples of how to use the various devices on the board. Also contains the pin assignments for the DP2 board.
- **Schematics**: The circuit diagrams and PCB layout for the DP2 board.
- **User manual**: The user manual for the DP2 board.

Should you have any problems reading the CD, the user manual and the datasheets are also available on-line at http://www.singmai.com/DP2.htm.
For other datasheets and the design files, please e-mail SingMai at enquiries@singmai.com.

Powering up DP2

DP2 requires a 9V DC power source at 2A which is connected via the jack socket J4, (see Figure 1). The board is supplied with a suitable AC-DC converter from SL power electronics, type no. PW173KA0903F01; a datasheet for this product is available on the DP2 web page.

The board is diode protected against the wrong polarity connection and also fused. Once powered up you should see four yellow diodes lit indicating the four on-board power supplies, 9V DC after the fuse and diode, 5VDC, 3.3VDC and 1.2VDC.

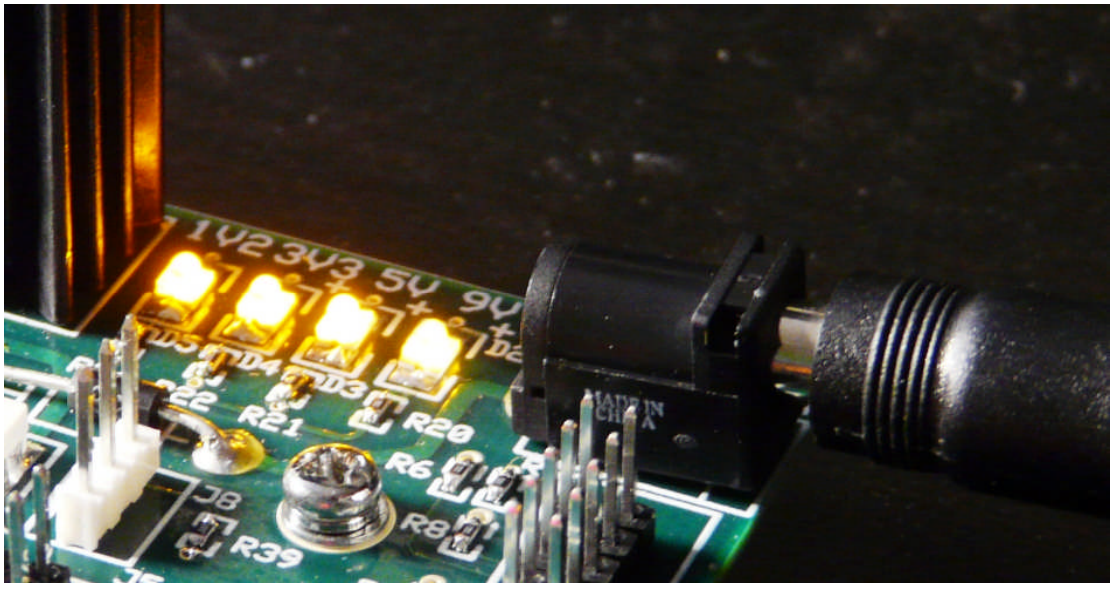

Figure 1 DC input connection

The 9VDC is used to derive the 5VDC and 3V3DC and also used for the LCD backlight if connected.
The 1V2DC is derived from the 3V3. All of the supplies are linear to provide the best signal to noise ratio for any ADCs and DACs.

The 5VDC is available at the expansion connectors J5 and J17 and is also used by the optical encoder, the USB interface, LCD display, optical audio transmitter and receiver and the TIL311 hexadecimal displays.

The 3V3 is also available at J5 and J17 and is used by the EEPROM, USB interface, crystal oscillator and for the I/O interfaces of the FPGA.
The 1V2 is available at the J6 expansion connector and is used for the core supply of the FPGA and the FPGA PLLs.

DP2 Mechanical layout

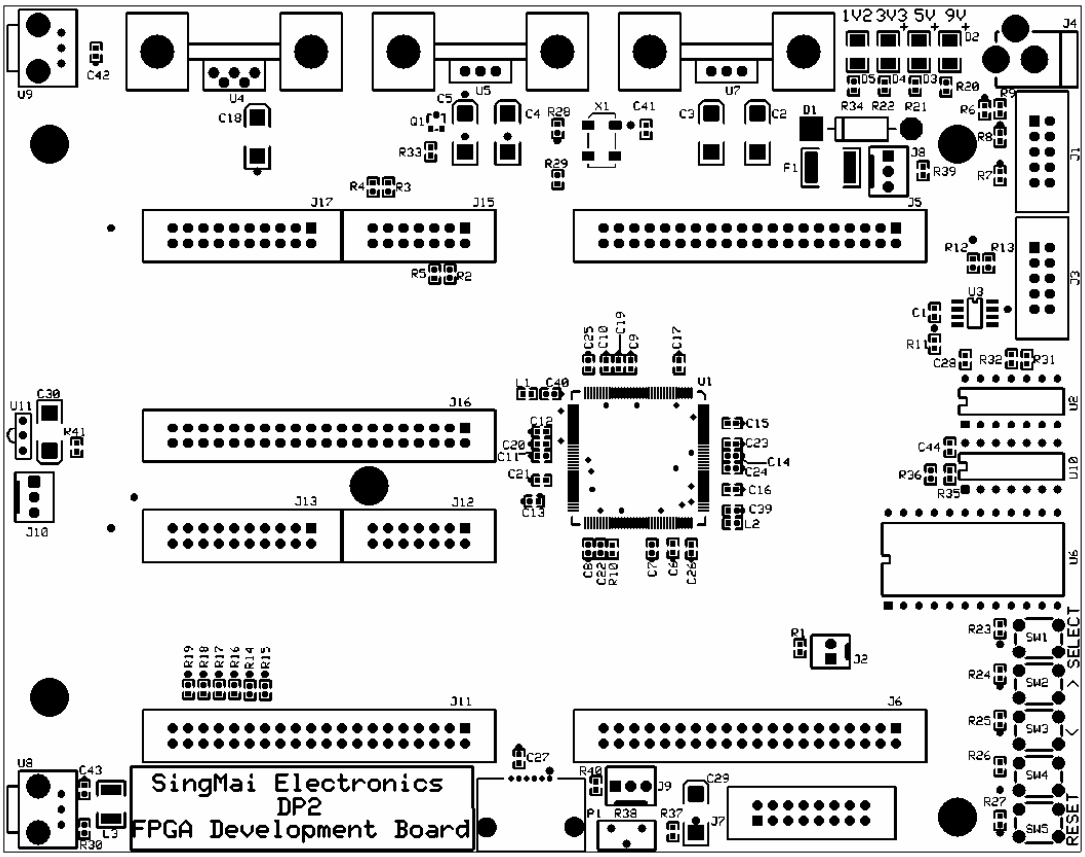

Figure 2 DP2 Mechanical layout

DP2 Parts List

The parts list for the DP2 is shown in Table 1, below.

Component ID	Value	Quantity	Type	Manufacturer
C1,C6-C17,C19-28,C39-C44	100nF	29	0603 Capacitor	Panasonic-ECG
C2-C5,C18,C29	47uF/16V	6	7343 SM Capacitor	Vishay_Sprague
D1	1N4001	1	Thro-board diode	Diodes Inc.
D2-D5	LED	4	1210 SM LED	Lite-on
F1	Fuse	1	6032 SM Fuse	LittleFuse
H1-H3	Heatsink	3	7-338-1PP	CTS Electronic Components
J1,J3	10W 5x2 0.1" header	2	90131-0125	Molex
J2	2W SIL 0.1" header	1	1-87215-0	Tyco Electronics
J4	Jack socket	1		CUI
J5,J6,J11,J15	40W 20x2 0.1" header	4	90131-0140	Molex
J7	16W 8x2 0.1" header	1	90131-0128	Molex
J12,J16	14W 7x2 0.1" header	2	90131-0127	Molex
J17	20W 10x2 0.1" header	1	90131-0130	Molex
L1,L2	Ferrite Bead	2	0603 Inductor	Panasonic-ECG
L3	47uH inductor	1	6032 SM inductor	Panasonic-ECG
P1	Optical encoder	1	16 pulse/rev encoder	Bourns
Q1	2N3904	1	SM NPN transistor	Infineon
R1,R6-R9	1k	5	0603 Resistor	Vishay-Dale
R2,R3	100R	2	0603 Resistor	Vishay-Dale
R4,R5,R33	3k3	3	0603 Resistor	Vishay-Dale
R10-R19,R23-R28,R30	10k	17	0603 Resistor	Vishay-Dale
R20	1k5	1	0603 Resistor	Vishay-Dale
R21,R31,R32,R35,R36	560R	5	0603 Resistor	Vishay-Dale
R22,R34	270R	2	0603 Resistor	Vishay-Dale
R29	33R	1	0603 Resistor	Vishay-Dale
R37	39R	1	0603 Resistor	Vishay-Dale
R38	10k	1	Side adjust potentiometer	Bourns
SW1-SW5	Pushbutton	5	6mm Push button (Omron B3F-1022, Digikey SW403-ND)	Omron
U1	EP2C8T144C8N	1	FPGA	Altera
U2,U10	TIL311	2	Hexadecimal display	TI
U3	EPCS4SI8	1	Serial EEPROM	Altera

Component ID	Value	Quantity	Type	Manufacturer
U4	UC382TD	1	1V2 TO220-5 regulator	TI
U5	LM1117	1	3V3 TO220 regulator	NSC
U6	DLP-USB245M	1	USB Interface	DLP Design
U7	LM1117	1	5V TO220 regulator	NSC
U8	TORX177	1	SPDIF receiver	Toshiba
U9	TOTX177	1	SPDIF transmitter	Toshiba
X1	27MHz oscillator	1	SG636 SM oscillator	Epson

Table 1 DP2 Part List

Technical description

The circuit diagrams for the DP2 can be found in the 'Schematics' directory on the CD.

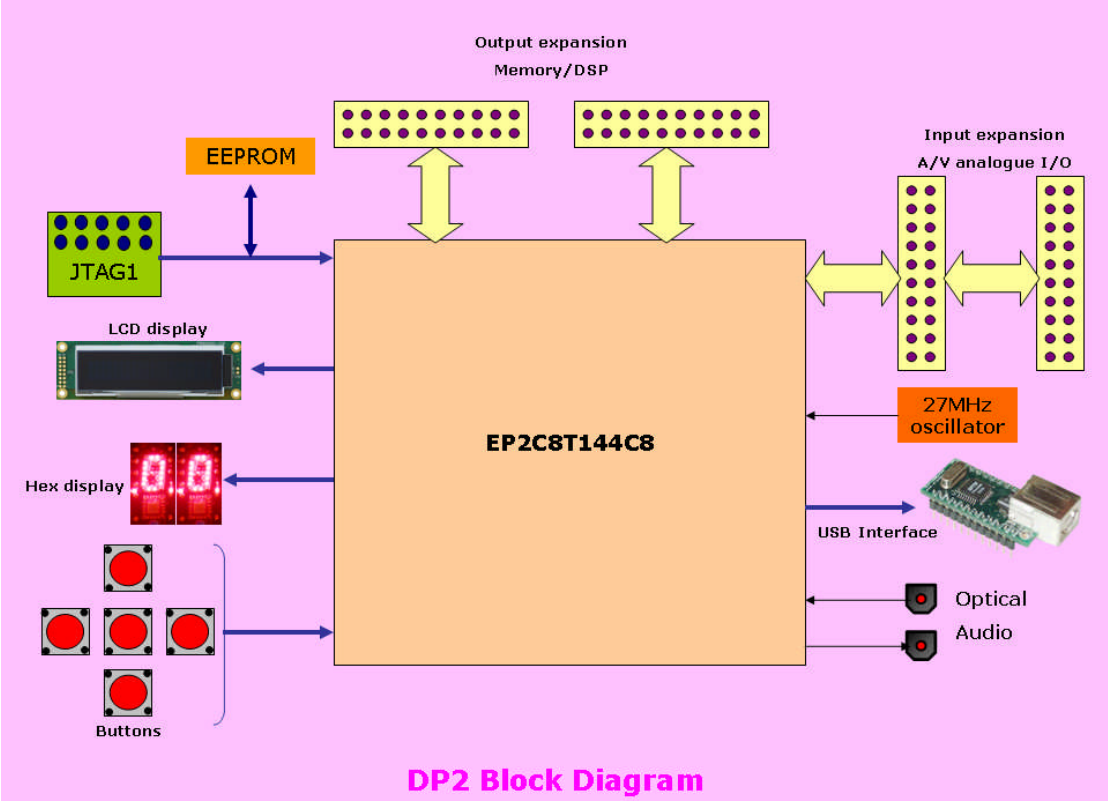

Figure 3 DP2 Block diagram

DP2 Test software

When the board is first powered up the FPGA is configured from the program stored in the on-board serial EEPROM. This program demonstrates the features of the board as follows.

Initially the two hexadecimal displays will show a seconds counter, from 0-59secs re-circulating. If the RESET button is pressed the count is reset to zero.

Pressing the SELECT pushbutton switches between the various display functions.

Pressing the button once will switch to the display of the value set by the two '<' and '>' buttons. These buttons produce an eight bit value that can be used to set values in your design. If the RESET button is pressed the count is reset to zero.

Pressing the button again will show a value corresponding to the digital encoder position. If the RESET button is pressed the count is reset to zero.

FPGA Pin outs

The EP2C8 on the DP2 card is provided in a cost effective 144 pin package which gives 85 user pins available. Because of this pin limitation some of the FPGA pins have a dual function. Table 2 lists the pin assignments, together with dedicated purpose, if connected to a board device, or their nominated purpose if used with the DP1 or DP3 expansion boards.

Pin No	Connection	Nominal Function
1	ASD0	See FPGA/EEPROM Programming information
2	nCSO	See FPGA/EEPROM Programming information
3	J16/39	Y_CVBS9 DP1 AD9981 Y/CVBS output
4	J16/37	Y_CVBS8 DP1 AD9981 Y/CVBS output
5	VCC_IO	3V3 supply
6	GND	
7	J16/35	Y_CVBS7 DP1 AD9981 Y/CVBS output
8	J16/33	Y_CVBS6 DP1 AD9981 Y/CVBS output
9	J16/31	Y_CVBS5 DP1 AD9981 Y/CVBS output
10	TDO	JTAG
11	TMS	JTAG
12	TCK	JTAG
13	TDI	JTAG
14	DATA0	See FPGA/EEPROM Programming information
15	DClk	See FPGA/EEPROM Programming information
16	nCE	See FPGA/EEPROM Programming information
17	J17/13	DataCk AD9981 Pixel clock output
18	SIN	Audio optical receiver input
19	GND	
20	nCONFIG	See FPGA/EEPROM Programming information
21	J16/29	Y_CVBS4 DP1 AD9981 Y/CVBS output
22	J16/27	Y_CVBS3 DP1 AD9981 Y/CVBS output
23	VCC_IO	3V3 supply
24	J16/25	Y_CVBS2 DP1 AD9981 Y/CVBS output
25	J16/23	Y_CVBS1 DP1 AD9981 Y/CVBS output
26	VCC_INT	1V2 supply
27	GND	
28	J16/21	Y_CVBS0 DP1 AD9981 Y/CVBS output
29	VCC_IO	3V3 supply
30	J16/17	CbCr9 DP1 AD9981 multiplexed Cb/Cr output
31	J16/15	CbCr8 DP1 AD9981 multiplexed Cb/Cr output
32	J16/13	CbCr7 DP1 AD9981 multiplexed Cb/Cr output
33	GND	
34	GND	
35	PLL1_VCCD	1V2 digital supply
36	GND	
37	PLL1_VDA	1V2 analog supply
38	GND	
39	GND	
40	J16/11	CbCr6 DP1 AD9981 multiplexed Cb/Cr output
41	J16/9	CbCr5 DP1 AD9981 multiplexed Cb/Cr output
42	J16/7	CbCr4 DP1 AD9981 multiplexed Cb/Cr output
43	J16/5	CbCr3 DP1 AD9981 multiplexed Cb/Cr output
44	J16/4	CbCr2 DP1 AD9981 multiplexed Cb/Cr output
45	J16/3	CbCr1 DP1 AD9981 multiplexed Cb/Cr output
46	VCC_IO	3V3 supply
47	J15/4	CbCr0 DP1 AD9981 multiplexed Cb/Cr output
48	J5/21	FIFO_SWCK
49	GND	
50	VCC_INT	1V2 supply
51	J11/39, J6/21	FIFO_SRCK output and DP1 output clock
52	J5/23	FIFO_RSTW output and USB_WR

Pin No	Connection	Nominal Function
53	J6/23, J7/6	FIFO_RSTR output and LCD display enable input
54	VCC_IO	3V3 supply
55	J5/25	FIFO_WE_1
56	GND	
57	J5/27	FIFO_WE_2 or USB RXF (selected by J8)
58	J6/25, J7/5	FIFO_RE_1 and LCD display R/W
59	J6/27, J7/4	LCD display R/W and either FIFO_RE_2 or USB TXE output (selected by J9)
60	EncoderB	Input from optical encoder
61	GND	
62	VCC_INT	1V2 supply
63	J11/27	Dual function out, HBlank to DP1/ SPDIF audio out to optical Tx
64	J15/8	VSOut_A0 AD9981 vertical sync output
65	J15/10	HSout AD9981 horizontal sync output
66	VCC_IO	3V3 supply
67	J5/1	FIFO_DIN9 output
68	GND	
69	J5/3	FIFO_DIN8 output
70	J5/5	FIFO_DIN7 output and U2 (Hex display) D3
71	J5/7	FIFO_DIN6 output and U2 (Hex display) D2
72	J5/9	FIFO_DIN5 output and U2 (Hex display) D1
73	J5/11	FIFO_DIN4 output and U2 (Hex display) D0
74	J5/13	FIFO_DIN3 output and U10 (Hex display) D7
75	J5/15	FIFO_DIN2 output and U10 (Hex display) D6
76	nCEO	Used as General I/O pin – USB_RDn
77	VCC_IO	3V3 supply
78	GND	
79	J5/17	FIFO_DIN1 output and U10 (Hex display) D5
80	GND	
81	VCC_INT	1V2 supply
82	nSTATUS	See FPGA/EEPROM Programming information
83	CONF_DONE	See FPGA/EEPROM Programming information
84	J2/2	MSel1, See FPGA/EEPROM programming information
85	MSel0	Connected to GND
86	J5/19	FIFO_DIN0 output and U10 (Hex display) D4
87	J12/5	DBClk Bit clock to audio DAC
88	XTAL_Clk	27MHz crystal clock input
89	J12/3	MClk input master clock from audio ADC
90	J12/9	ABClk input bit clock from audio ADC
91	J12/8	ASData1 input data from audio ADC
92	J12/7	ALR Clk output L/R clock to audio ADC
93	J12/4	DSData1 Output data to audio DAC
94	J12/6	DLRClk output L/R clock to audio DAC
95	VCC_IO	3V3 supply
96	J11/3	Y9 output
97	J11/4	Y8 output
98	GND	
99	J11/5	Y7 output
100	J11/6	Y6 output
101	J11/7	Y5 output
102	VCC_IO	3V3 supply
103	J11/8	Y4 output
104	J11/9	Y3 output
105	GND	
106	GND	
107	PLL2_VCCD	1V2 digital supply
108	GND	
109	PLL2_VDA	1V2 analog supply
110	GND	
111	GND	
112	J11/10	Y2 output
113	J11/11	Y1 output
114	J11/12	Y0 output
115	J15/5, J5/31	SDA I2C data
116	VCC_IO	3V3 supply
117	GND	
118	J15/13, J5/32	SCL I2C clock

Pin No	Connection	Nominal Function
119	J6/1	FIFO_DOUT9 input
120	J6/3	FIFO_DOUT8 input
121	J6/5	FIFO_DOUT7 input
122	J6/7	FIFO_DOUT6 input
123	GND	
124	VCC_INT	1V2 supply
125	J6/9	FIFO_DOUT5 input
126	J6/11	FIFO_DOUT4 input
127	VCC_IO	3V3 supply
128	GND	
129	J6/13	FIFO_DOUT3 input
130	GND	
131	VCC_INT	1V2 supply
132	J6/15	FIFO_DOUT2 input
133	J6/17	FIFO_DOUT1 input
134	J6/19	FIFO_DOUT0 input
135	SW4	Pushbutton input 4
136	SW3	Pushbutton input 3
137	SW2	Pushbutton input 2
138	VCC_IO	3V3 supply
139	SW1	Pushbutton input 1
140	GND	
141	SW0	Pushbutton input 0
142	EncoderA	Input from optical encoder
143	J15/12	OEField AD9981 Frame output
144	LED_Data_Stb	Latch data output to hexadecimal displays

Table 2 DP2 FPGA Pin Assignments

Expansion connector 1

There are two sets of expansion board connectors available on DP2 which may be split, for example to accommodate DP1 and DP3 or expansion boards of your own design, or for one larger board.
The mechanical layout for the first set of connectors is shown in Figure 5 and the connector pin-outs are shown in Tables 3 to 8.

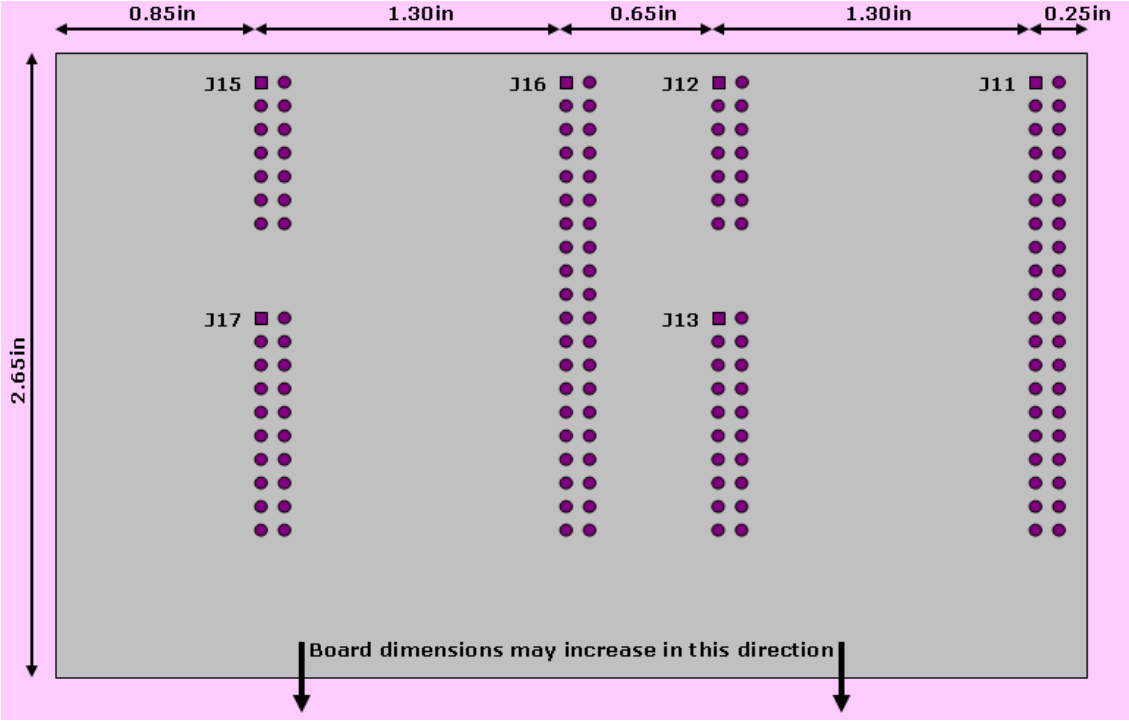

Figure 4 Expansion board 1 mechanical information

Pin No	Connection	Nominal Function
1	Not connected	
2	GND	
3	FPGA pin 44	Input/Output (LVDS75p)
4	Not connected	
5	FPGA pin 43	Input/Output (LVDS76n)
6	Not connected	
7	FPGA pin 42	Input/Output (LVDS76p)
8	Not connected	
9	FPGA pin 41	Input/Output (LVDS77p)
10	Not connected	
11	FPGA pin 40	Input/Output (LVDS77n)
12	Not connected	
13	FPGA pin 32	Input/Output (PLL1_OUTn)
14	Not connected	
15	FPGA pin 31	Input/Output (PLL1_OUTp)
16	Not connected	
17	FPGA pin 30	Input/Output
18	Not connected	
19	GND	
20	Not connected	
21	FPGA pin 28	Input/Output
22	GND	

Pin No	Connection	Nominal Function
23	FPGA pin 25	Input/Output (LVDS7n)
24	GND	
25	FPGA pin 24	Input/Output (LVDS7p)
26	GND	
27	FPGA pin 22	Input (LVDSCLK1n/input)
28	Not connected	
29	FPGA pin 21	Input (LVDSCLK1p/input)
30	GND	
31	FPGA pin 9	Input/Output (LVDS8n)
32	Not connected	
33	FPGA pin 8	Input/Output (LVDS8p)
34	GND	
35	FPGA pin 7	Input/Output
36	Not connected	
37	FPGA pin 4	Input/Output (LVDS15n)
38	Not connected	
39	FPGA pin 3	Input/Output (LVDS15p)
40	GND	

Table 3 J16 Pin-outs

Pin No	Connection	Nominal Function
1	Not connected	
2	GND	
3	FPGA pin 96	Input/Output (LVDS46p)
4	FPGA pin 97	Input/Output (LVDS45n)
5	FPGA pin 99	Input/Output
6	FPGA pin 100	Input/Output (LVDS39n)
7	FPGA pin 101	Input/Output (LVDS39p)
8	FPGA pin 103	Input/Output (PLL2_OUTp)
9	FPGA pin 104	Input/Output (PLL2_OUTn)
10	FPGA pin 112	Input/Output (LVDS37n)
11	FPGA pin 113	Input/Output (LVDS37p)
12	FPGA pin 114	Input/Output (LVDS36n)
13	Not connected	
14	Not connected	
15	Not connected	
16	Not connected	
17	Not connected	
18	Not connected	
19	GND	
20	Not connected	
21	Not connected	
22	GND	
23	Not connected	
24	GND	
25	Not connected	
26	GND	
27	FPGA pin 63	Input/Output. Also connected to optical audio output
28		10k resistor to 3V3
29		10k resistor to 3V3
30	GND	
31		10k resistor to GND
32		10k resistor to GND
33		10k resistor to GND
34	GND	
35		10k resistor to GND
36	Not connected	
37	Not connected	
38	Not connected	
39	FPGA pin 51	Input/Output. Also connected to J6/21
40	GND	

Table 4 J11 Pin-outs

Pin No	Connection	Nominal Function
1	GND	
2	Not connected	
3	Not connected	
4	FPGA pin 47	Input/Output (LVDS74p)
5	FPGA pin 115	Input/Output (LVDS36p). 3k3 pullup to 3V3 and 100R series resistor to FPGA. FPGA also connected to J5/31
6	Not connected	
7	Not connected	
8	FPGA pin 64	Input/Output (LVDS60p)
9	Not connected	
10	FPGA pin 65	Input/Output (LVDS60n)
11	Not connected	
12	FPGA pin 143	Input/Output (LVDS16p)
13	FPGA pin 118	Input/Output (LVDS34n). 3k3 pullup to 3V3 and 100R series resistor to FPGA. FPGA also connected to J5/32
14	Not connected	

Table 5 J15 Pin-outs

Pin No	Connection	Nominal Function
1	Not connected	
2	Not connected	
3	FPGA pin 89	Input (LVDSCLK3p/input)
4	FPGA pin 93	Input/Output (LVDS47p)
5	FPGA pin 87	Input/Output (LVDS48p)
6	FPGA pin 94	Input/Output (LVDS46n)
7	FPGA pin 92	Input/Output (LVDS47n)
8	FPGA pin 91	Input (LVDSCLK2p/input)
9	FPGA pin 90	Input (LVDSCLK2n/input)
10	Not connected	
11	Not connected	
12	Not connected	
13	Not connected	
14	GND	

Table 6 J12 Pin-outs

Pin No	Connection	Nominal Function
1	9V	
2	GND	
3	Not connected	
4	GND	
5	3V3	
6	GND	
7	3V3	
8	GND	
9	Not connected	
10	GND	
11	Not connected	
12	GND	
13	FPGA pin 17	Input (LVDSCLK0p/input)
14	GND	
15	Not connected	
16	GND	
17	5V	
18	GND	
19	5V	
20	GND	

Table 7 J17 Pin-outs

Pin No	Connection	Nominal Function
1	9V	
2	GND	

Pin No	Connection	Nominal Function
3	Not connected	
4	GND	
5	3V3	
6	GND	
7	3V3	
8	GND	
9	Not connected	
10	GND	
11	Not connected	
12	GND	
13	Not connected	
14	GND	
15	Not connected	
16	GND	
17	5V	
18	GND	
19	5V	
20	GND	

Table 8 J13 Connector Pin-out

Expansion connector 2

The mechanical layout for the second set of connectors is shown in Figure 6 and the connector pin-outs are shown in Tables 9 and 10.

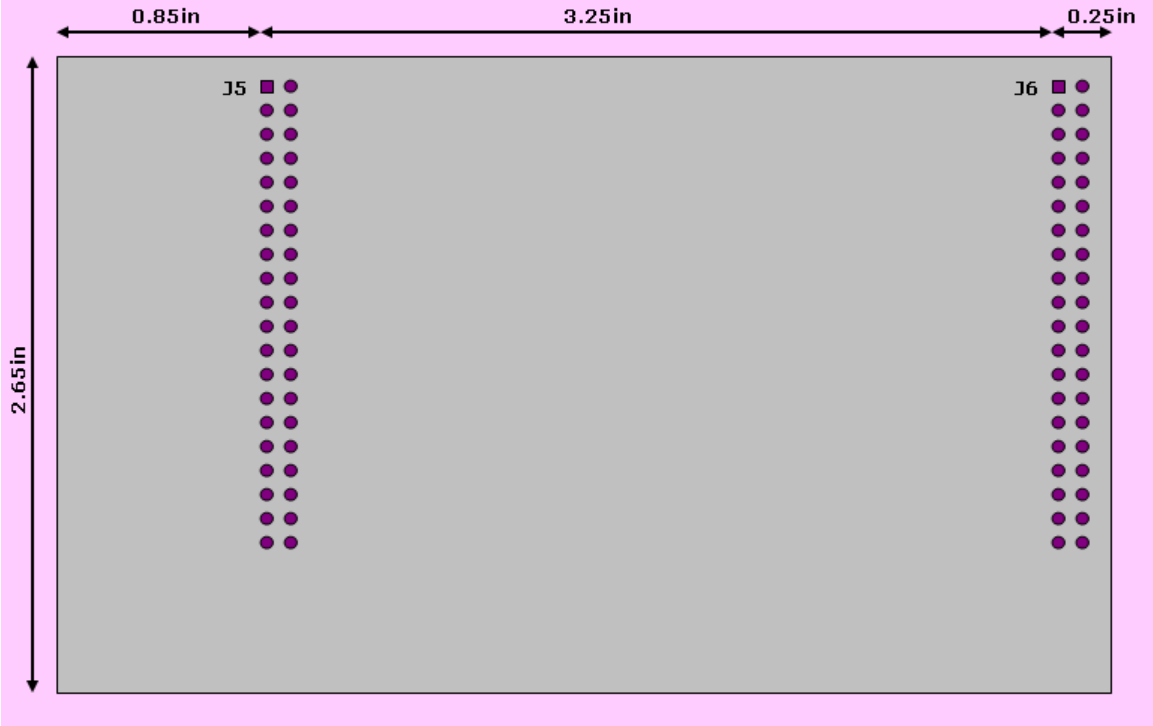

Figure 5 Expansion connector 2 Mechanical layout

Pin No	Connection	Nominal Function
1	FPGA pin 67	Input/Output (LVDS59n)
2	GND	
3	FPGA pin 69	Input/Output (LVDS58p)
4	GND	
5	FPGA pin 70	Input/Output (LVDS58n)
6	GND	
7	FPGA pin 71	Input/Output (LVDS57p)
8	GND	
9	FPGA pin 72	Input/Output (LVDS57n)
10	GND	
11	FPGA pin 73	Input/Output (LVDS56n)
12	GND	
13	FPGA pin 74	Input/Output (LVDS56p). Also connected to U10 Data D
14	GND	
15	FPGA pin 75	Input/Output (LVDS54n). Also connected to U10 Data C
16	GND	
17	FPGA pin 79	Input/Output. Also connected to U10 Data B
18	GND	
19	FPGA pin 86	Input/Output (LVDS48n). Also connected to U10 Data A
20	GND	
21	FPGA pin 48	Input/Output (LVDS74n)
22	GND	
23	FPGA pin 52	Input/Output (LVDS70p). Also connected to USB WR
24	GND	
25	FPGA pin 55	Input/Output (LVDS68n)
26	GND	
27	J8/1	3k3 pull-up to 3V3
28	GND	

Pin No	Connection	Nominal Function
29	27MHz	Crystal oscillator output
30	GND	
31	FPGA pin 115	Input/Output (LVDS36p). Also 100R series resistor and 3k3 pull-up to 3V3 to J5/5.
32	FPGA pin 118	Input/Output (LVDS34n). Also 100R series resistor and 3k3 pull-up to 3V3 to J5/13.
33	3V3	
34	3V3	
35	3V3	
36	3V3	
37	Not connected	
38	Not connected	
39	5V	
40	5V	

Table 9 J5 Connector Pin-out

Pin No	Connection	Nominal Function
1	FPGA pin 119	Input/Output (LVDS34p)
2	GND	
3	FPGA pin 120	Input/Output
4	GND	
5	FPGA pin 121	Input/Output (LVDS33n)
6	GND	
7	FPGA pin 122	Input/Output (LVDS33p)
8	GND	
9	FPGA pin 125	Input/Output (LVDS29n)
10	GND	
11	FPGA pin 126	Input/Output (LVDS29p)
12	GND	
13	FPGA pin 129	Input/Output (LVDS26p)
14	GND	
15	FPGA pin 132	Input/Output.
16	GND	
17	FPGA pin 133	Input/Output (LVDS23n).)
18	GND	
19	FPGA pin 134	Input/Output (LVDS23p).)
20	GND	
21	FPGA pin 51	Input/Output. Also connected to J11/39
22	GND	
23	FPGA pin 53	Input/Output (LVDS68p). Also connected to J7/6.
24	GND	
25	FPGA pin 58	Input/Output (LVDS67n). Also connected to J7/5.
26	GND	
27	J9/1	3k3 pull-up to 3V3
28	GND	
29	Not connected	
30	Not connected	
31	Not connected	
32	Not connected	
33	Not connected	
34	Not connected	
35	1V2	
36	1V2	
37	1V2	
38	1V2	
39	1V2	
40	1V2	

Table 10 J6 Connector Pin-out

Programming the FPGA and EEPROM

Two configurations schemes for the FPGA can be used on the DP2 development board.
Connector J1 supports JTAG configuration. The pin-outs for this connector are shown in Table 11.

Pin No	Connection	Nominal Function
1	FPGA pin 12	TCK. 1k resistor to GND
2	GND	
3	FPGA pin 10	TDO.
4	3V3	
5	FPGA pin 11	TMS. 1k resistor to 3V3
6		1k resistor to 3V3
7	Not connected	
8	Not connected	
9	FPGA pin 13	TDI. 1k resistor to 3V3
10	GND	

Table 11 J1 JTAG connector pinouts

J1 may be connected to ByteBlaster II, MasterBlaster, USB-Blaster or ByteBlaster MV download cables. JTAG configuration takes priority over the other configuration schemes. A *.sof file should be used as the FPGA configuration file. To download the supplied DP2_Test configuration file you should see a screen similar to the one below.

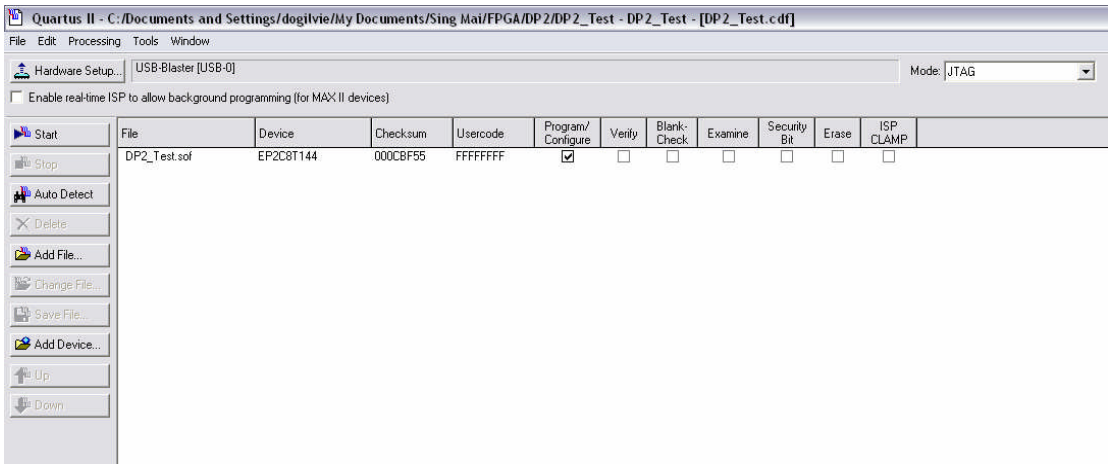

Figure 6 Programming the FPGA using the JTAG interface

J3 also connects to the ByteBlaster or USB-Blaster download cables. This connector allows programming of the on-board EEPROM which enables the FPGA to be automatically configured on power-up using Active Serial mode, and gives DP2 a standalone capability. The pin-outs for J3 are shown in Table 12.

Pin No	Connection	Nominal Function
1	FPGA pin 15	DCLK to FPGA and EEPROM
2	GND	

Pin No	Connection	Nominal Function
3	FPGA pin 83	CONF_DONE. 10k resistor to 3V3
4	3V3	
5	FPGA pin 20	nCONFIG. 10k resistor to 3V3
6	FPGA pin 16	nCE. 10k resistor to GND
7	FPGA pin 14	DATA0 to FPGA and EEPROM
8	FPGA pin 2	nCSO to FPGA and EEPROM
9	FPGA pin 1	ASDO to FPGA and ASDI to EEPROM
10	GND	

Table 12 Active serial configuration connector pin-outs

The EEPROM is a EPCS4SI8; a datasheet can be found on the DP2 web page. To program the EEPROM you need to create a *.pof programming file. In the FPGA device assignment menu set the configuration to 'Active serial' and set the configuration device to be EPCS4.

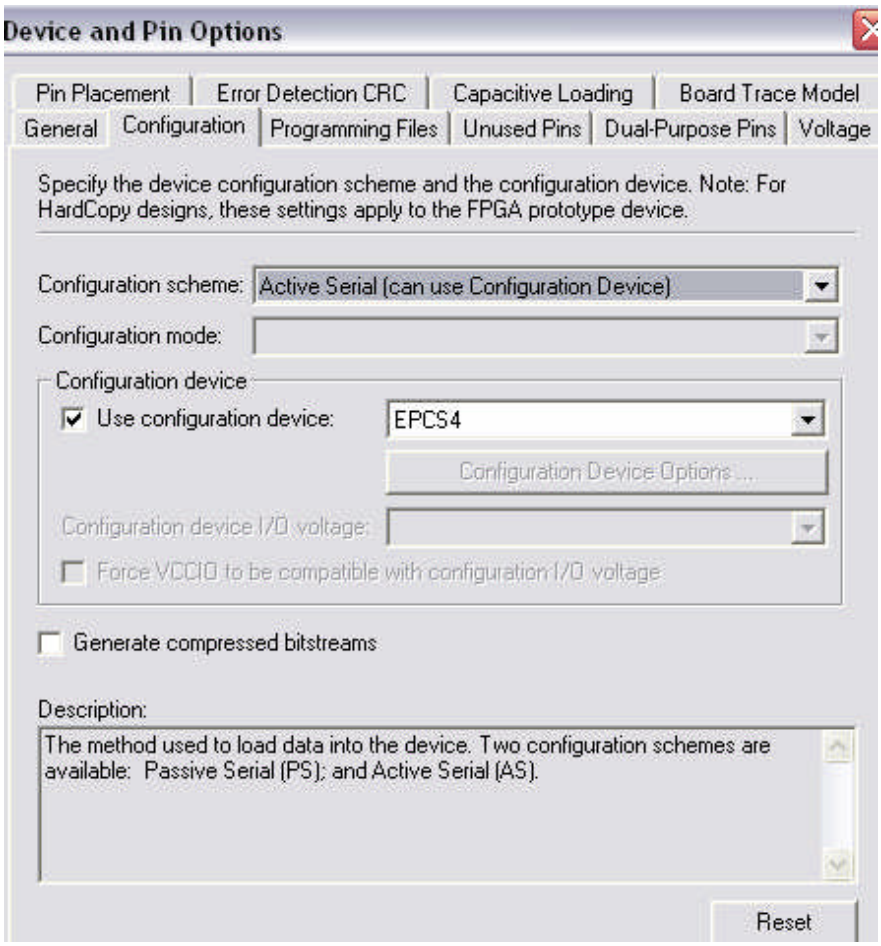

Figure 7 Setting the device configuration for the EEPROM

When you compile the program a *.pof file be automatically created which can be selected by the programmer for downloading to the EEPROM. Once this is done then the FPGA will automatically configure itself on switch on from the EEPROM allowing standalone operation. Downloading a new program from the JTAG connector will over-write the EEPROM configuration file.

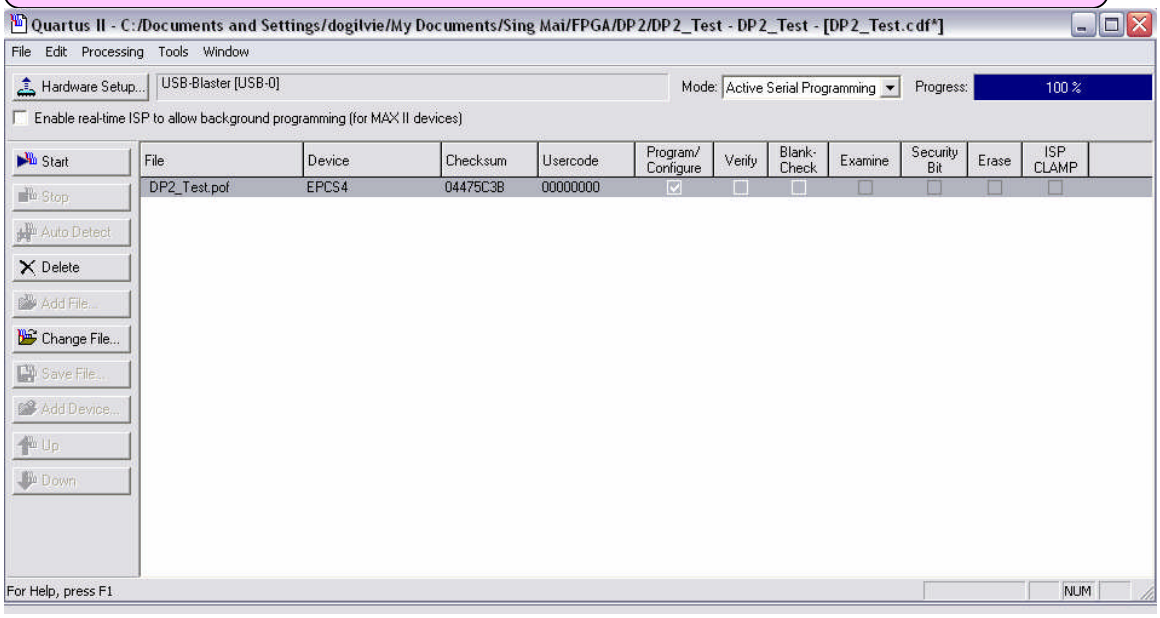

Figure 8 Programming the EEPROM

The Hexadecimal Displays

Two Texas Instruments TIL311 hexadecimal displays are provided, U2, (least significant) and U10, (most significant). The displays accepts 8-bit binary data from the FPGA which can be optionally latched to the displays and which is displayed as two hexadecimal digits, 0-F.

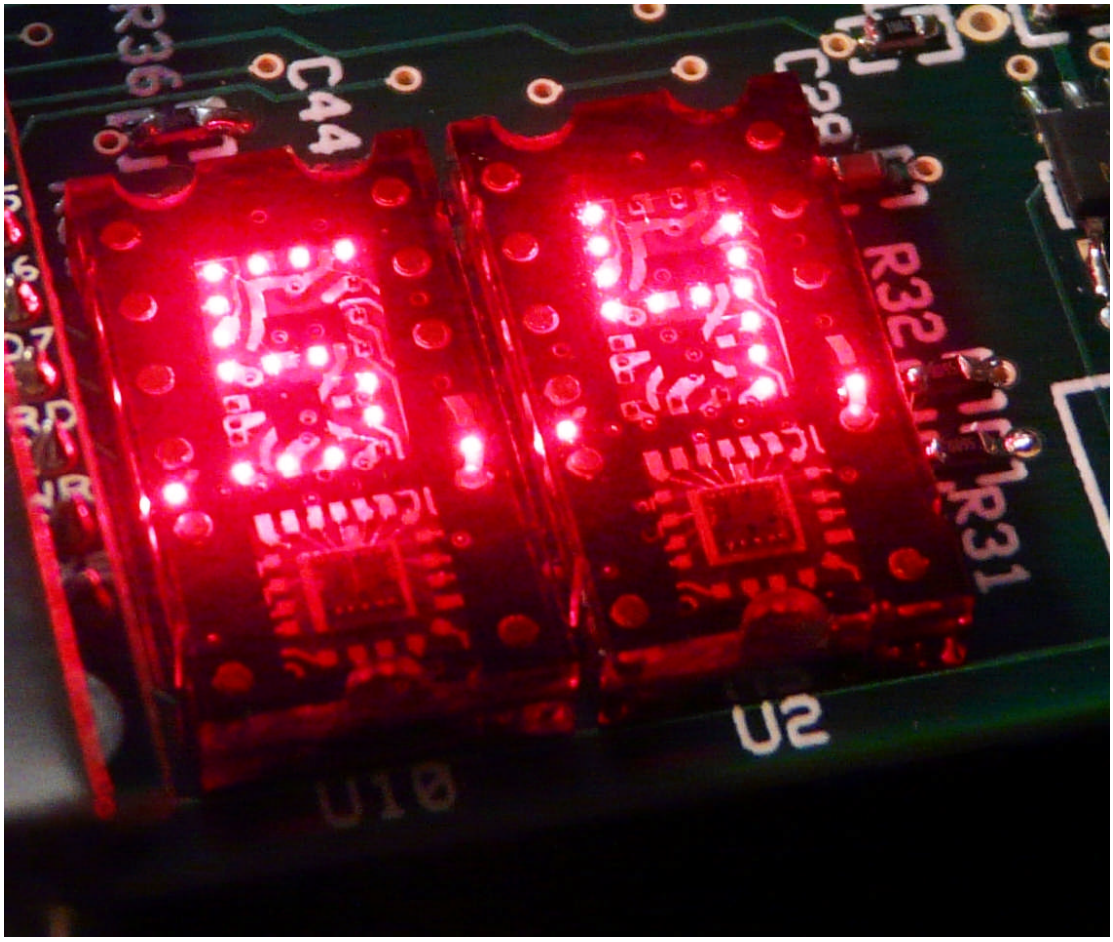

Figure 9 The hexadecimal displays

A data sheet on the TIL311 can be found on the DP2 web page. The connections to the displays are shown in Table 13. Note that these pins are also shared with expansion connector J5, the USB interface, U6, and the LCD display, connector J7.

FPGA Pin No	Connection	Nominal Function
73	Hex_display[0]	D0 (U2 bit A)
72	Hex_display[1]	D0 (U2 bit B)
71	Hex_display[2]	D0 (U2 bit C)
70	Hex_display[3]	D0 (U2 bit D)
86	Hex_display[4]	D0 (U10 bit A)
79	Hex_display[5]	D0 (U10 bit B)
75	Hex_display[6]	D0 (U10 bit C)
74	Hex_display[7]	D0 (U10 bit D)
144	LED_Data_Stb	Latches data to display on low to high transition. Holding this input low makes the LED latches

FPGA Pin No	Connection	Nominal Function
		transparent.

Table 13 Hexadecimal display connections

Driving the displays is very straightforward as shown by the AHDL code below.

```
--      ********************************************************************
--      Output data to Hexadecimal displays
        HEX_display[7..0] = (Seconds_MSD.q[3..0],Seconds_LSD.q[3..0]);
--      Set the Hexadecimal display latches to trasnparent mode
        LED_Data_Stb = GND;
```

The outputs Hex_display[7..0] and LED_Data_stb correspond with the outputs shown in Table 13.
In this example the LED latches are made transparent so any data presented to them is immediately displayed. The example above displays a 0-59 second counter from the counters shown in the section on the crystal oscillator. If you are using the data bus (Hex_display[7..0]) for the other functions it is recommended that you use the LED latches to hold the data. Note when doing this the setup and hold requirements for the latch strobe.

The USB interface

DP2 includes a USB interface which is provided by the DLP-USB245M interface, a datasheet of which is available on the DP2 webpage. The connections to this interface are shown in Table 15.

FPGA Pin No	Connection	Nominal Function
86	Hex_display[4]	USB databus D0
79	Hex_display[5]	USB databus D1
75	Hex_display[6]	USB databus D2
74	Hex_display[7]	USB databus D3
73	Hex_display[0]	USB databus D4
72	Hex_display[1]	USB databus D5
71	Hex_display[2]	USB databus D6
70	Hex_display[3]	USB databus D7
76	USB_RDn	USB read enable. Note that this pin is a dual purpose pin for the FPGA and to use it, it is necessary to set the dual purpose pin assignment to 'use as regular I/O'.
52	USB_WRn	USB write enable. This pin is shared with expansion connector J5 pin 23.
59	USB_TXE	USB transmit buffer empty. J9 must be linked pins 2-3. This FPGA pin is also connected to J7 pin 4 (LCD display).
57	USB_RXF	USB Receive buffer full. J8 must be linked pins 2-3.

Table 14 USB interface connections

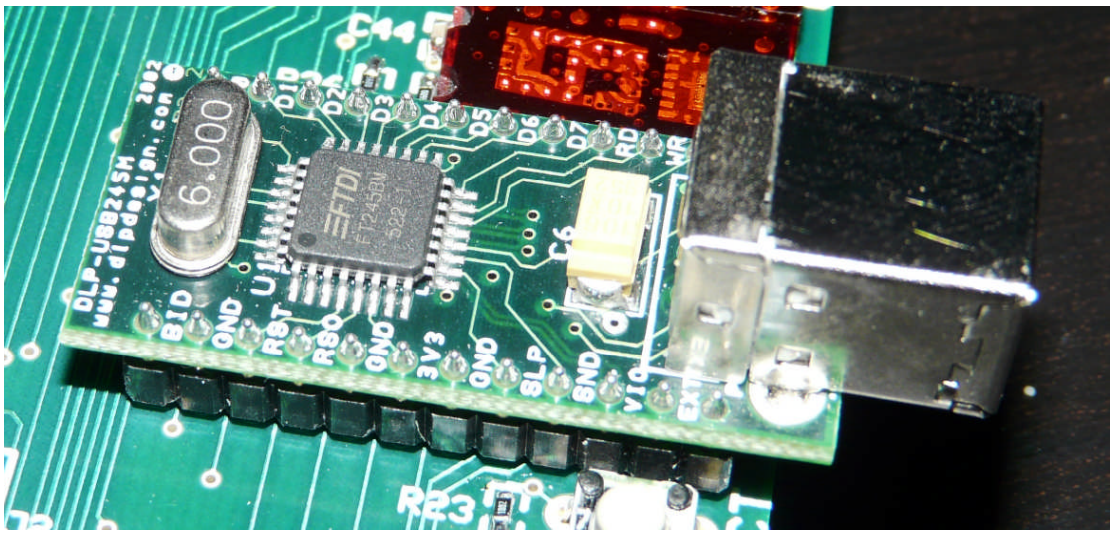

Figure 10 USB interface

The LCD display

The connections for the DP2 are shown in Figure 3, below.

The Optical Encoder

The DP2 board incorporates a Bourns' optical encoder. This device is convenient for the analog control of digital functions. A datasheet on the device is available on the DP2 web page.

There are two quadrature outputs from the encoder allow both position and direction of the control to be evaluated.

The AHDL code below generates an 8-bit value, Encoder_count.q[7..0], that may be used for control purposes.

```
--      Optical encoder
        Encoder_Dir                             :       lpm_ff with (lpm_width=1);
        Encoder_count                   :       lpm_counter with (lpm_width=8);

--      Read Optical encoder
--      Optical encoder interface
        Encoder_Dir.(data[], clock) = (EncoderB, EncoderA);
--      Encoder Direction low for CW and high for CCW
        Encoder_count.(clock, updown, aclr) = (EncoderB, !Encoder_Dir.q[], !RESETn);
```

The Push buttons

Five push-to-make pushbuttons are provided on DP2. Each button has a 10k pull-up resistor to the 3.3V power rail and pushing the button pulls this to ground. The buttons can be used for any purpose but are nominally dedicated on the board's legend to provide reset, up/down and select functions.

The switch connections are shown in Table 14.

FPGA Pin No	Connection	Nominal Function
141	SW0	Switch SW1, input grounded when switch pressed
139	SW1	Switch SW2, input grounded when switch pressed
137	SW2	Switch SW3, input grounded when switch pressed
136	SW3	Switch SW4, input grounded when switch pressed
135	SW4	Switch SW5, input grounded when switch pressed

Table 15 Pushbutton switch connections

For reliable operation the buttons should be de-bounced to ensure a clean output. This AHDL demonstrates how to do that for the momentary reset switch, SW5.

```
--      Pushbutton switches
        Button_debounce_1ms                     lpm_constant with (lpm_width=16,
                                                lpm_cvalue=27000);
        Button_latch9                   :       lpm_ff with (lpm_width=1);
        Button_latch10                  :       lpm_ff with (lpm_width=1);
        Button_debounce_count_4         :       lpm_counter with (lpm_width=16);
        Button_debounce_time_4          :       lpm_compare with (lpm_width=16,
        lpm_pipeline=0, one_input_is_constant="yes");

--      Button 4 Momentary button (RESET)
        Button_latch9.(data[],clock) = (!SW[4], XTAL_27MHz);
        Button_latch10.(data[],clock) = (Button_latch9.q[], XTAL_27MHz);
        Button_debounce_count_4.(clock, cnt_en, aclr) = (XTAL_27MHz,
        !Button_debounce_count_4.q[15],
                (Button_latch9.q[] and !Button_latch10.q[]));
        Button_debounce_time_4.(dataa[], datab[]) = (Button_debounce_count_4.q[15..0],
                Button_debounce_1ms.result[]);
        RESETn = Button_debounce_count_4.q[15];
```

The Crystal Oscillator

A 27.000MHz crystal oscillator is provided on the DP2 development board. The pin connections are shown in Table 17.

FPGA Pin No	Connection	Nominal Function
88	XTAL_clk	27MHz crystal clock input: dedicated FPGA clock input.

Table 16 Crystal oscillator connections

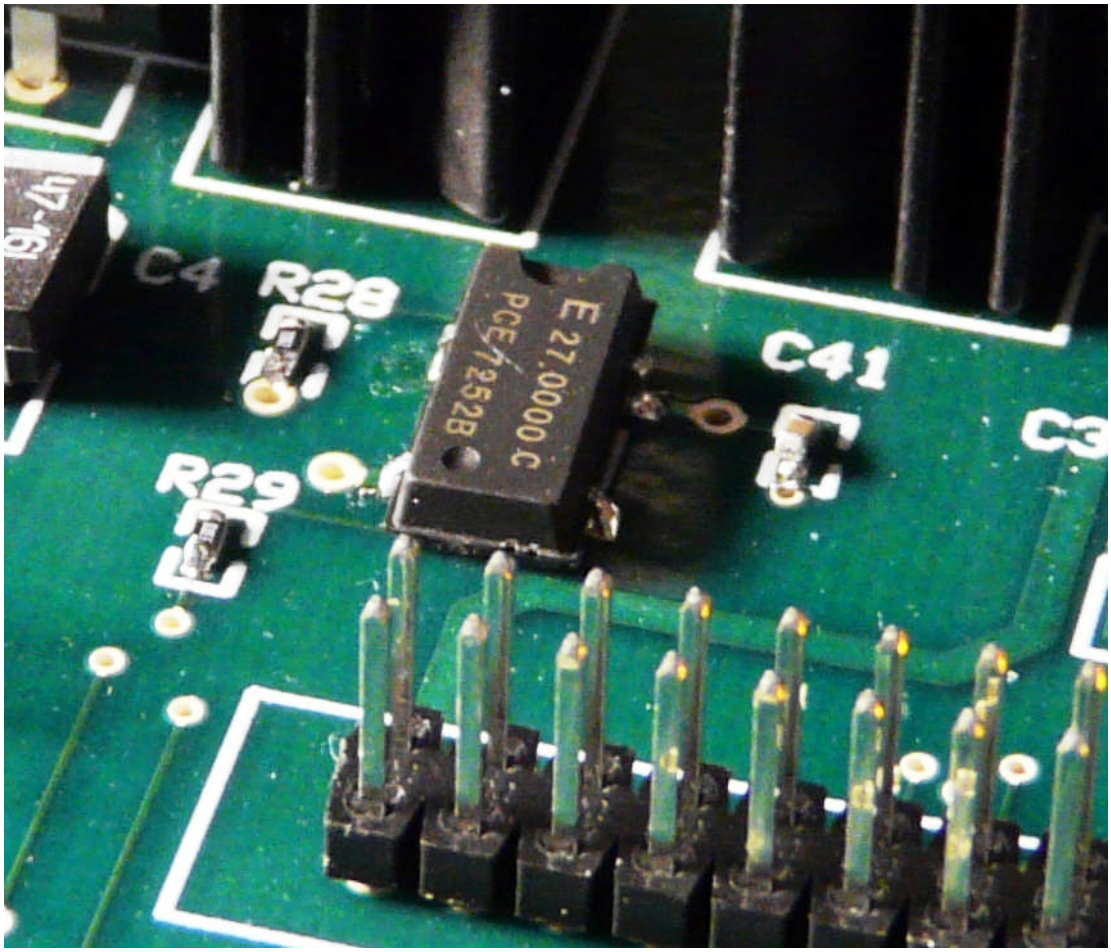

Figure 11 Crystal oscillator

The AHDL code example below shows the oscillator being used to generate a seconds display. The section on the hexadecimal displays shows how to display this.

```
--      Seconds counter
        Divider                                 :       lpm_counter with (lpm_width=25);
        Divider_value                           :       lpm_constant with (lpm_width=25,
        lpm_cvalue=27000000);
        Divider_compare                         :       lpm_compare with (lpm_width=25,
        lpm_pipeline=0, one_input_is_constant="yes");
        Seconds_LSD                             :       lpm_counter with (lpm_width=4);
        Seconds_LSD_value                       :       lpm_constant with (lpm_width=4,
        lpm_cvalue=9);
        Seconds_LSD_compare                     :       lpm_compare with (lpm_width=4,
        lpm_pipeline=0, one_input_is_constant="yes");
        Seconds_MSD                             :       lpm_counter with (lpm_width=4);
```

```
        Seconds_MSD_value                       :       lpm_constant with (lpm_width=4,
        lpm_cvalue=5);
        Seconds_MSD_compare                     :       lpm_compare with (lpm_width=4,
        lpm_pipeline=0, one_input_is_constant="yes");

--      Generate 1 second clicks from 27MHz crystal
        Divider.(clock, sclr) = (XTAL_clk, Divider_compare.aeb);
        Divider_compare.(dataa[], datab[]) = (Divider.q[24..0], Divider_value.result[]);

--      Count 1 second clicks in BCD. Counters can be reset by using the RESETn, SW5 pushbutton
        switch
        Seconds_LSD.(clock, cnt_en, sclr, aclr) = (XTAL_clk, Divider_compare.aeb,
                                                                (Seconds_LSD_compare.aeb
        and Divider_compare.aeb), !RESETn);
        Seconds_LSD_compare.(dataa[], datab[]) = (Seconds_LSD.q[3..0],
        Seconds_LSD_value.result[]);
        Seconds_MSD.(clock, cnt_en, sclr, aclr) = (XTAL_clk, (Divider_compare.aeb and
        Seconds_LSD_compare.aeb),
                                (Seconds_MSD_compare.aeb and Divider_compare.aeb and
        Seconds_LSD_compare.aeb), !RESETn);
        Seconds_MSD_compare.(dataa[], datab[]) = (Seconds_MSD.q[3..0],
        Seconds_MSD_value.result[]);
```

The infra-red receiver

The conne

The optical audio transmitter/receiver

The connections for the DP2 are shown in Figure 3, below.