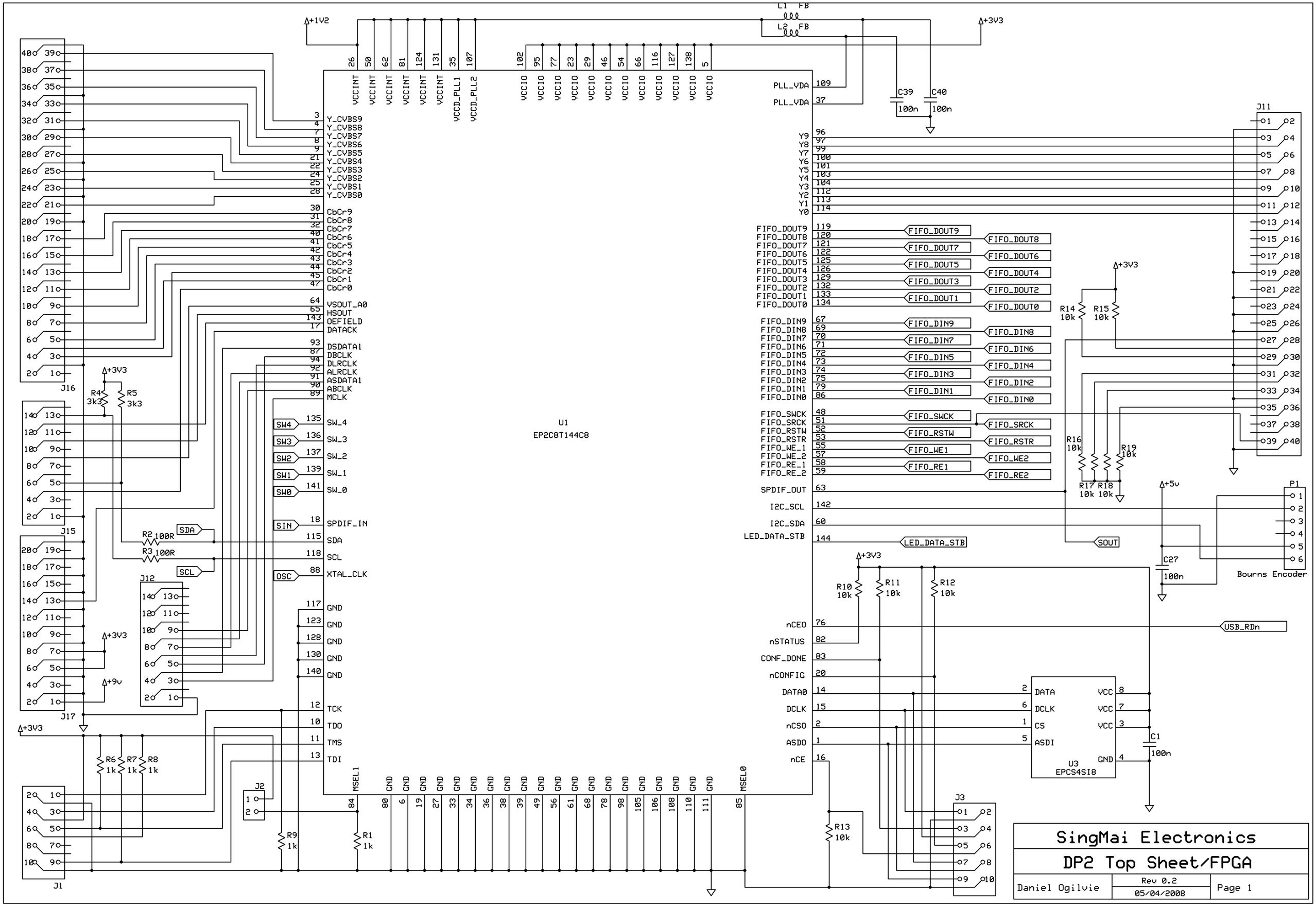
U1
EP2C8T144C8
U3
EPCS4SI8
J11
P1
Bourns Encoder
J16
J15
J12
J17
J1
J2
J3
+1V2
+3V3
+5v
+9v
L1 FB
L2 FB
C39 100n
C40 100n
C27 100n
C1 100n
R1 1k
R2 100R
R3 100R
R4 3k3
R5 3k3
R6 1k
R7 1k
R8 1k
R9 1k
R10 10k
R11 10k
R12 10k
R13 10k
R14 10k
R15 10k
R16 10k
R17 10k
R18 10k
R19 10k
SW4
SW3
SW2
SW1
SW0
SIN
OSC
SDA
SCL
SOUT
USB_RDn
LED_DATA_STB
Y_CVBS9
Y_CVBS8
Y_CVBS7
Y_CVBS6
Y_CVBS5
Y_CVBS4
Y_CVBS3
Y_CVBS2
Y_CVBS1
Y_CVBS0
CbCr9
CbCr8
CbCr7
CbCr6
CbCr5
CbCr4
CbCr3
CbCr2
CbCr1
CbCr0
VSOUT_A0
HSOUT
OEFIELD
DATACK
DSDATA1
DBCLK
DLRCLK
ALRCLK
ASDATA1
ABCLK
MCLK
SW_4
SW_3
SW_2
SW_1
SW_0
SPDIF_IN
SDA
SCL
XTAL_CLK
GND
TCK
TDO
TMS
TDI
MSEL1
MSEL0
VCCINT
VCCD_PLL1
VCCD_PLL2
VCCIO
PLL_VDA
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
FIFO_DOUT9
FIFO_DOUT8
FIFO_DOUT7
FIFO_DOUT6
FIFO_DOUT5
FIFO_DOUT4
FIFO_DOUT3
FIFO_DOUT2
FIFO_DOUT1
FIFO_DOUT0
FIFO_DIN9
FIFO_DIN8
FIFO_DIN7
FIFO_DIN6
FIFO_DIN5
FIFO_DIN4
FIFO_DIN3
FIFO_DIN2
FIFO_DIN1
FIFO_DIN0
FIFO_SWCK
FIFO_SRCK
FIFO_RSTW
FIFO_RSTR
FIFO_WE_1
FIFO_WE_2
FIFO_RE_1
FIFO_RE_2
SPDIF_OUT
I2C_SCL
I2C_SDA
LED_DATA_STB
nCEO
nSTATUS
CONF_DONE
nCONFIG
DATA0
DCLK
nCSO
ASDO
nCE
DATA
DCLK
CS
ASDI
VCC
GND
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DP2 Top Sheet/FPGA
Daniel Ogilvie
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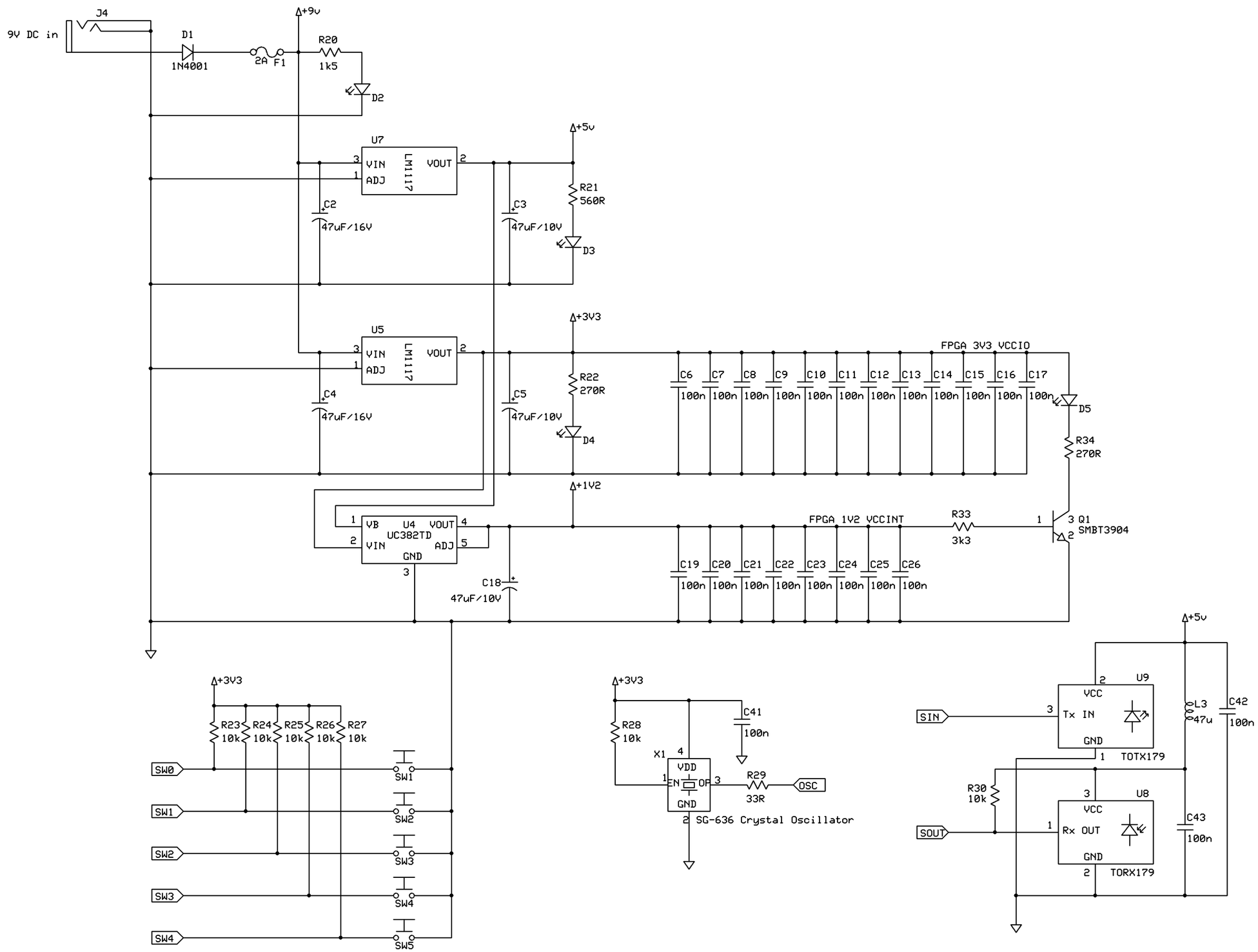
Page 1



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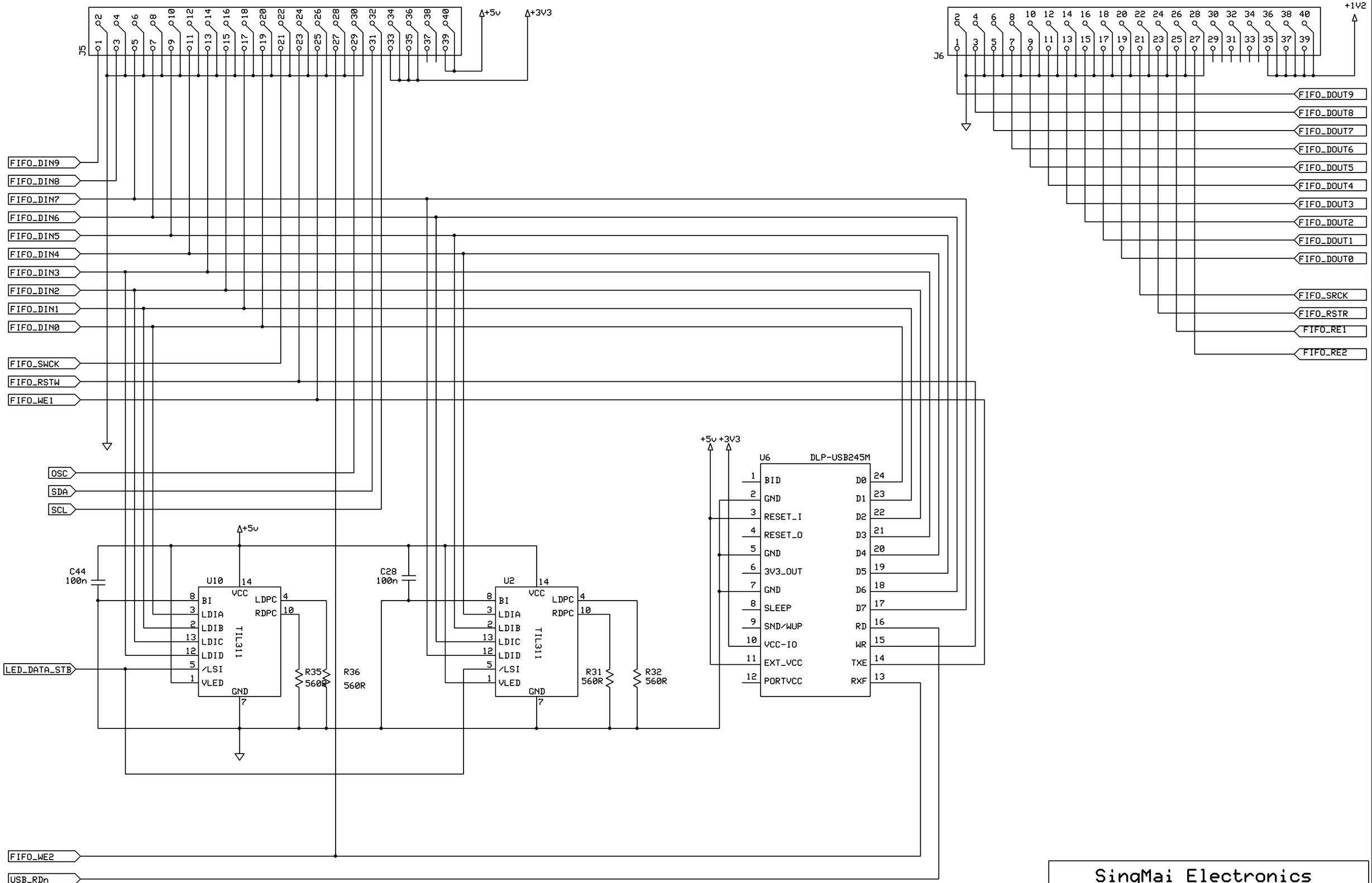

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DP2 Expansion connector		
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