PT3

User Manual

NTSC Video Decoder

Revision 0.1
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Introduction

PT3 is a PAL Video encoder. The decoder accepts 10-bit composite line locked video sampled at 27MHz together with synchronising signals and clock, (for example from the Analog Devices AD9981 ADC). The decoder is a complementary design. The colour burst from the input video is used to phase lock the subcarrier oscillator which then addresses a sine and cosine LUT. These waveforms are used to demodulate the colour component of the composite waveform. The resulting U and V colour components are then low pass filtered and applied to a 3-line adaptive comb filter. The chrominance comb adapts between a notch filter and the line comb based on the chrominance and luminance amplitude differences across the comb aperture. The resulting combed U and V components provide the colour component outputs where they are amplified and scaled before being formatted to a 10-bit BT656 output. The combed U and V are also remodulated onto the colour subcarrier and subtracted from the composite to produce a combed luminance output which is also scaled and formatted into the BT656 stream.
Control and status registers are written to and read from using a conventional 8 bit wide microprocessor interface.

The intellectual property block is provided as an encrypted 'black box' design for incorporation into an Altera FPGA, either for stand-alone operation or for integration with other blocks. The resources required are shown in Table 1.

Logic Elements	Memory Bits	M4K blocks	9x9 Multipliers	18x18 multipliers

Table 1 FPGA resource requirements

Signal Interconnections

The PT3 signal interconnect diagram is shown in Figure 1.

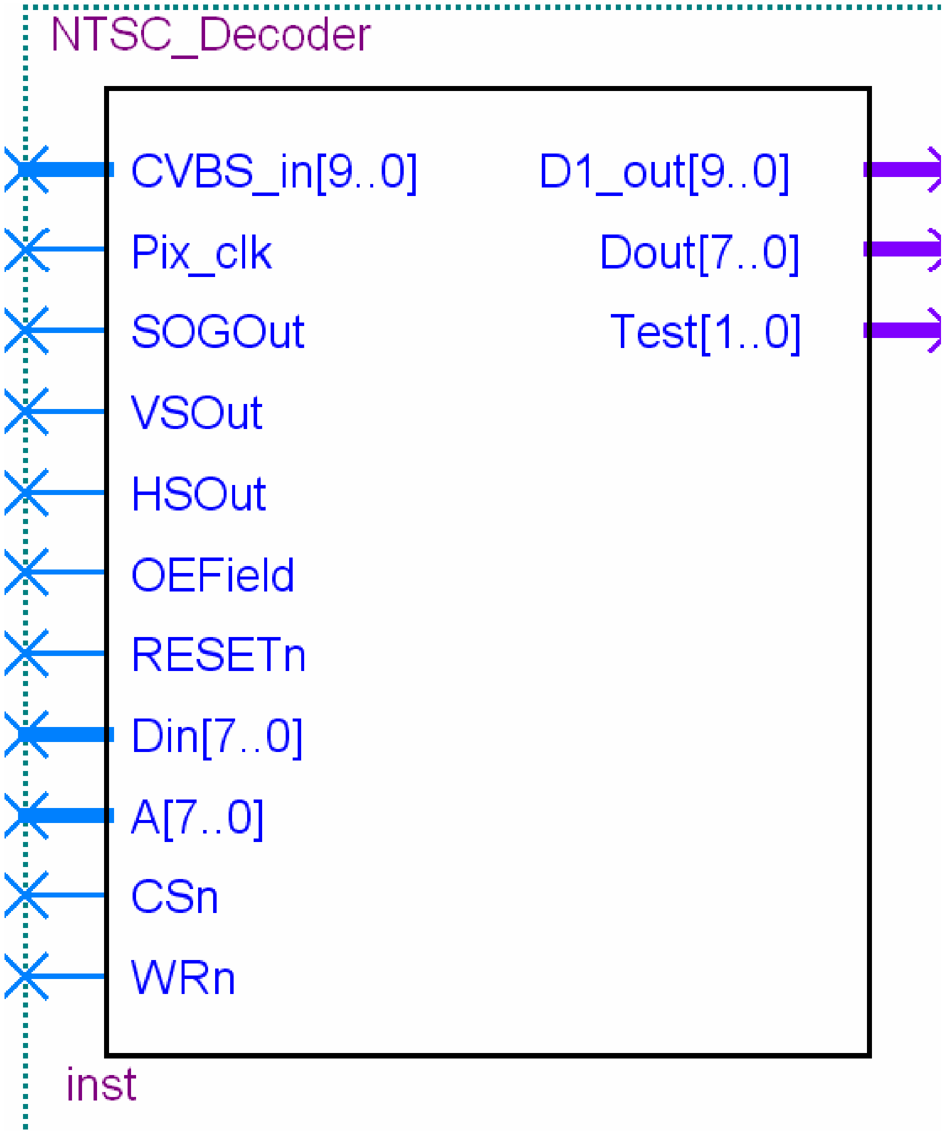

Figure 1 PT3 Signal Interconnects

The signal descriptions are shown in Table 2, below.

Signal	Description
CVBS_in[9..0]	Digitised composite video input. If the input is 8-bits the bottom 2 bits should be wired to ground.
Pix_clk	27MHz clock input synchronous with the composite input data, (CVBS_in[9..0]. The composite data should be stable at the rising edge of this clock.

SOGOut	The raw sync-on-green output from the AD9981. This input is only used for status information.
VSOut	The extracted vertical sync pulse from the incoming CVBS signal. Connects to the VSout/A0 pin of the AD9981.
HSOut	The extracted horizontal sync pulse, (i.e. with field group removed), from the incoming CVBS signal. Connects to the HSout pin of the AD9981.
OEField	The field identifier output of the AD9981. The odd/even polarity may be switched within the IP core. Connects to the HSout pin of the AD9981.
RESETn	Active low reset signal. Asserting this input sets all the control registers to their default value.
Din[7..0]	Control data input bus.
A[7..0]	Control address bus input used to select the control register to be written to/read from.
CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers.
D1_out[9..0]	The 10-bit, BT656 formatted output video, synchronous with the input 27MHz clock, Pix_clk.
Dout[7..0]	Control output data bus. Outputs the control/status register data selected by the A[7..0] bus.
Test[1..0]	Used in combination with the test control register to select internal test signals.

Table 2 Input/Output signals

The Altera include file is shown below:

```
FUNCTION NTSC_Decoder (CVBS_in[9..0], Pix_clk, SOGOut, VSOut,
HSOut, OEField, RESETn, Din[7..0], A[7..0], CSn, WRn)
        WITH (LPM_WIDTHS)
        RETURNS (D1_out[9..0], Dout[7..0], Test[1..0]);
```

An example of using the include file within a design is shown here.

Interfacing to the AD9981

The PT3 decoder can is designed to seamlessly interface to the Analog Devices AD9981 video front end, but it may also be interfaced to other front end designs. The signals the PT3 core requires broadly fall into two groups, timing and data.

If not using the AD9981, the timing information required can be provided by a sync separator IC such as the Gennum GS4982, (http://www.gennum.com/video/products/gs4982.htm).

The Vertical Sync, Horizontal Sync and Odd/Even outputs of the GS4982 drive the VSout, HSout and OEField inputs of the IP block directly. Timing differences between the sync positions, the polarity of the OEField input, the input CVBS signal and the final BT656 formatted output can be offset within the IP core using programmable registers

The AD9981 contains an integrated sync separator but it does not have a subcarrier rejection filter. This means the burst and other chrominance information on the composite input disrupts the recovered sync. To avoid this an external sync filter must be added. This is shown in Figure 2.

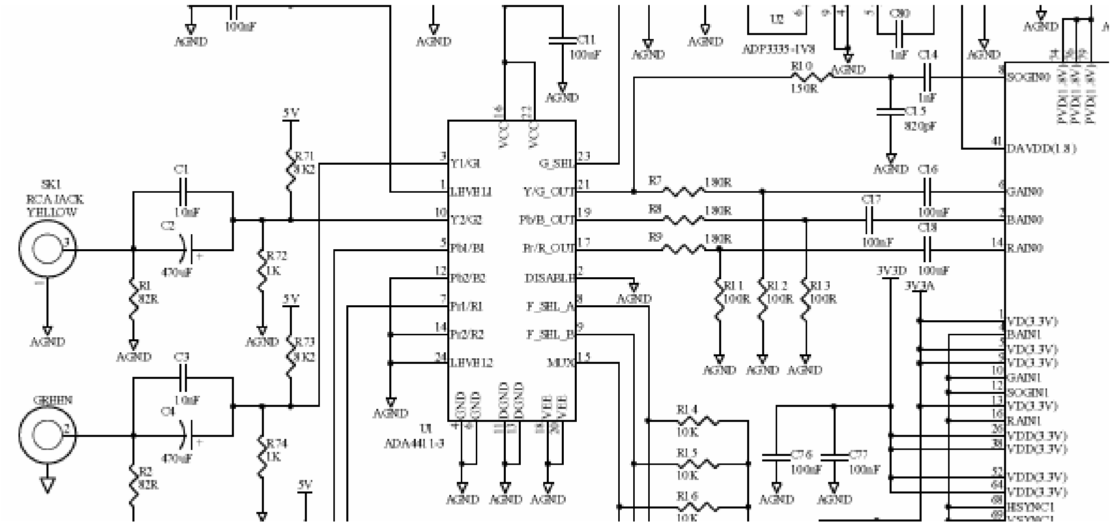

Figure 2 AD9981 interface

This is an example of the AD9981 interface used on the DP1 interface card. (http://www.singmai.com/DP1.htm).

The composite video input is applied to SK1. It is terminated, AC coupled and then DC offset to match the input requirements of the Analog devices AD4411-3. This devices provides a x2 gain and a programmable filter that is used as an anti-aliasing filter. The output of this drives the Gain0 (Green) input of the AD9981. Because the maximum input signal of the AD9981 is 1V pk-pk and the composite input exceeds this (nominal pk-pk signal of 1.26V for

100% colour bars), we must attenuate the input which is the function of the 180R/100R resistor network.
The composite video is also filtered by the 150R/820pF combination to remove the subcarrier from the input to the sync separator. The resulting digital composite video output appears on the Green[9..0] outputs.
The AD9981 provides the timing signals and also provides clamping and gain controls for the video. It also provides a line locked clock which is programmed to be 27MHz. If a discrete front end is being used this clock will have to be derived by another method.

The register settings for the AD9981 are shown in Table 3.

Address	Register Name	Register Value									Description
		7	6	5	4	3	2	1	0	Hex	
0x00	Chip Revision	0	0	0	0	0	0	0	0	00	Chip revision: Read only
0x01	PLL Div MSB	0	1	1	0	1	0	1	1	6B	1716 Pixels/line
0x02	PLL Div LSB	0	1	0	0	0	0	0	0	40	
0x03	VCO/CPMP	0	1	1	0	0	0	0	0	60	VCO range=1, Charge Pump=4, Use internal PLL
0x04	Phase Adjust	1	0	0	0	0	0	0	0	80	
0x05	Red Gain MSBs	0	1	1	1	1	1	1	1	40	
0x06	Red Gain LSBs	0	0	0	0	0	0	0	0	00	
0x07	Green Gain MSBs	0	1	1	1	1	1	1	1	58	
0x08	Green Gain LSBs	0	0	0	0	0	0	0	0	00	
0x09	Blue Gain MSBs	0	1	1	1	1	1	1	1	40	
0x0A	Blue Gain LSBs	0	0	0	0	0	0	0	0	00	
0x0B	Red Offset MSBs	0	1	0	0	0	0	0	0	40	Auto Offset mode used
0x0C	Red Offset LSBs	0	0	0	0	0	0	0	0	00	
0x0D	Green Offset MSBs	0	0	0	0	0	0	0	0	16	Auto Offset mode used
0x0E	Green Offset LSBs	1	0	0	0	0	0	0	0	80	
0x0F	Blue Offset MSBs	0	1	0	0	0	0	0	0	40	Auto Offset mode used
0x10	Blue Offset LSBs	0	0	0	0	0	0	0	0	00	
0x11	Sync Separator Threshold	0	0	1	0	0	0	0	0	20	
0x12	Hsync control	1	1	0	0	0	0	0	0	C0	Sync source=SOG
0x13	Hsync Duration	0	1	1	1	1	1	1	1	7F	
0x14	Vsync control	1	1	0	0	0	1	1	0	C6	Vsync filter enabled
0x15	Vsync duration	0	0	0	0	1	0	1	0	0A	
0x16	Precoast	0	0	0	0	0	1	0	0	04	
0x17	Postcoast	0	0	0	0	0	1	0	0	04	
0x18	Coast and Clamp control	0	0	0	0	1	0	1	0	0A	Internal clamp, YPbPr clamping levels
0x19	Clamp Placement	0	0	0	0	0	1	0	0	04	
0x1A	Clamp duration	0	0	0	1	0	1	0	0	14	
0x1B	Clamp and Offset	0	0	1	1	0	0	1	1	33	Auto offset mode
0x1C	Testreg0	1	1	1	1	1	1	1	1	FF	
0x1D	SOG control	0	1	1	1	1	0	0	0	60	
0x1E	Power	1	0	0	1	0	1	0	0	94	Channel 0 selected, low bandwidth
0x1F	Output select 1	1	0	0	1	0	0	0	0	90	4:4:4 10 bit mode
0x20	Output select 2	0	0	0	0	0	1	1	1	07	Use filtered sync

		Register Value									
0x21		0	1	0	0	0	0	0	0	**20**	
0x22		0	0	1	1	0	0	1	0	**32**	
0x23	Sync filter window width	0	0	0	1	0	1	0	0	**14**	
0x24	Sync detect	0	0	0	0	1	0	0	0	**08**	Read only
0x25	Sync polarity detect	0	1	1	0	1	1	1	1	**6F**	Read only
0x26	Hsyncs per Vsync MSB	0	0	0	1	0	0	0	0	**10**	Read only
0x27	Hsyncs per Vsync LSB	0	1	1	1	0	0	0	0	**70**	Read only
0x28	Testreg1	1	0	1	1	1	1	1	1	**BF**	Must be written with $BF
0x29	Testreg2	0	0	0	0	0	0	0	0	**02**	
0x2A	Testreg3	0	0	0	0	0	0	0	0	**00**	Read only
0x2B	Testreg4	0	0	0	0	0	0	0	0	**00**	Read only
0x2C	Offset hold	0	0	0	0	0	0	0	0	**00**	Update auto-offset
0x2D	Testreg5	1	1	1	0	1	0	0	0	**E8**	
0x2E	Testreg6	1	1	1	0	0	0	0	0	**E0**	

Table 3 AD9981 register settings for use with the PT3 IP core

Signal Levels

The typical input codes for a 100% colour bar input, (Green[9..0] output of the AD9981) are shown in Figure 4.

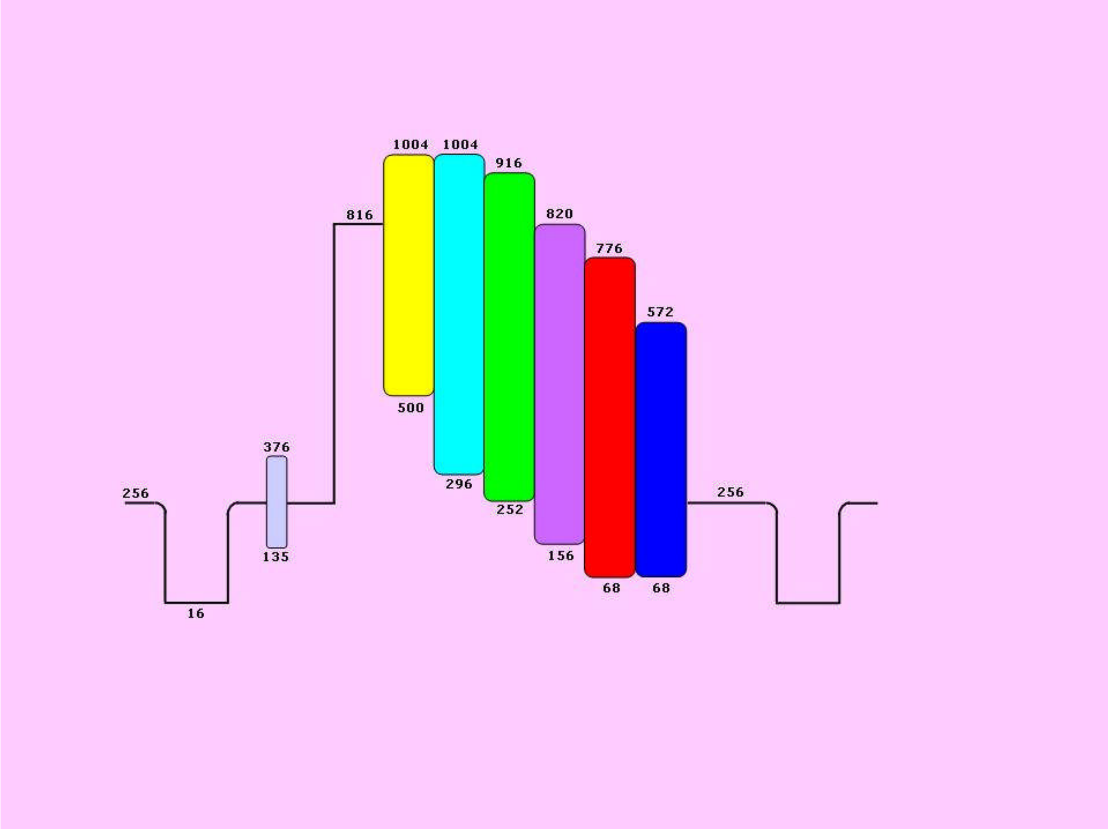

Figure 3 Input CVBS codes

The resulting expected signal levels for the PT3 BT656 output are shown in Table 3, below.

10-bit YCbCr signal Levels 100/0/100/0			
	Y	**Cb**	**Cr**
White	940	512	512
Yellow	840	64	585
Cyan	678	663	64
Green	578	215	137
Magenta	426	809	887
Red	326	361	960
Blue	164	960	439
Black	64	512	512

Table 4 BT656 Output Signal Levels

Technical Overview

A simplified block diagram of the PT3 NTSC decoder is shown in Figure 5.

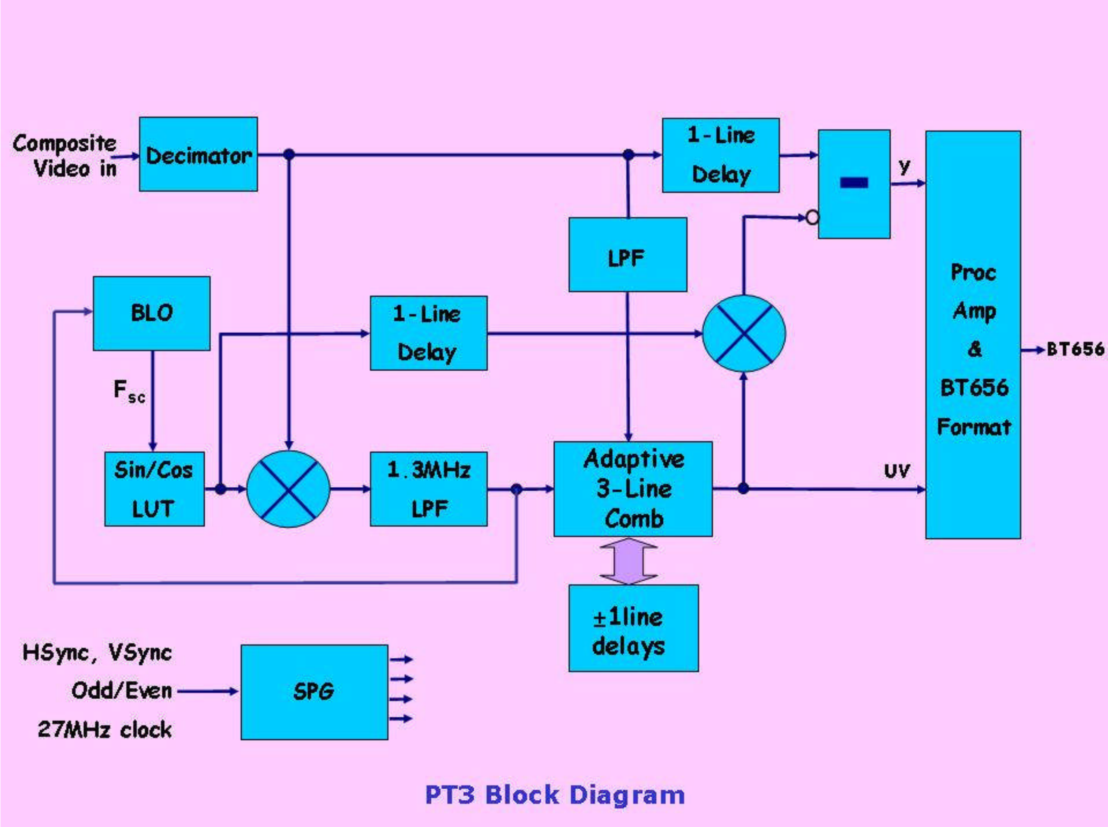

Figure 4 PT3 Block Diagram

The input to the decoder is 10 bit digitised composite, (CVBS), video at a 27MHz sample rate.
The clock and the extracted synchronizing signals are sent to the sync pulse generator. In turn this generates all of the required internal timing signals as well as the flags required for the BT656 compliant output. A phase locked loop also generates a 54MHz clock which is used for multiplexing of internal multipliers to reduce the IP core requirements.
The 27MHz composite video is first filtered and decimated to 13.5MHz. The filter has a pass band response of +/-0.3dB to 6MHz whist ensuring sufficient attenuation to avoid aliasing components. The resulting video is then fed to two multipliers. The other input to one of the multipliers is a Sin waveform, the other a Cos waveform. The waveforms are derived from a ROM which is addressed by the phase word of a burst locked oscillator, BLO, running at a nominal 3.58MHz, the NTSC subcarrier frequency. The resulting output from the two multipliers is the demodulated chrominance signal and also a twice frequency component. The latter is removed by a 1.3MHz

low-pass filter. The output of this filter is the 'simple' U and V components. A sample of these components during the colour burst is sent back to close the loop for the BLO.
The 'simple' U and V components and then filtered in a 3 line comb. Matching delays to the centre point of the comb are also provided for the Sin/Cos waveforms and the CVBS video. The output of the comb is either a delayed version of the 'simple U/V or a line combed version. Switching between these outputs is done using a comb adaptation circuit which analyses the Y,U and V signals across the taps of the comb to detect when the line comb would fail. Switching is performed on a pixel rate basis. The CVBS signal into the comb adaptation circuit is filtered to remove the chrominance component.
The resulting 'clean' U and V is fed to the Processing amplifier and BT656 formatter whilst also being multiplied by the delayed Sin and Cos waveforms and added together to form a reconstituted chrominance component. This is then subtract from the delayed CVBS signal to leave a combed luminance signal, which again is sent to the Proc. Amp and BT656 formatter.
The Proc amp level shifts and scales the Y, U and V to the Y, Cb and Cr level requirements of the final BT656 output. TRS codes are added to the final multiplexed, BT656, output.
Control of the PT3 IP core is via a 'standard' 8 bit microprocessor style control bus. Registers are addressed using a 6 bit wide address bus and written to using chip select and write enable signals. The control registers offer a read back facility and in addition status registers provide monitoring of the status of the decoder. Two test outputs allow a choice of internal timing signals to be output.

Control Interface

The following table l

Register descriptions

The following table lists all of the control and status registers. All of the registers are 8 bit wide although some are concatenated together to create longer words. Asserting the RESETn input sets all the registers to their default values. Unused bits read back as '0's.

Register Offset	Register Name	R/W	Bit Value	Default Value	Description
					Version number
$00	**Version No.**	R		1	IP Version number
					SPG
$01	**H Back Porch 2**	R/W		1	Delay between falling edge of recovered Hsync ,(HSn), and start of active video. Increments of 1/27MHz. 9 bit value = (HBackPorch2[0],HBackPorch1[7..0]).
$02	**H Back Porch 1**	R/W		6	
$03	**Active video start 2**	R/W		0	Delay HBackPorch value and BT656 active video start, effectively the horizontal delay through the decoder. Increments of 1/27MHz. 11 bit value = (Activevideostart2[2..0],Activevideostart1[7..0]).
$04	**Active video start 1**	R/W		50	
$05	**Active video end 2**	R/W		5	End of BT656 active video pulse. Must be set to Active video start value + 1440. Increments of 1/27MHz. 11 bit value = (Activevideoend2[2..0],Activevideoend1[7..0]).
$06	**Active video end 1**	R/W		210	
$07	**Burst Gate start**	R/W		102	Start position of the burst gate pulse used to sample to demodulated chrominance output. Increments of 1/13.5MHz. 8 bit value = BurstGatestart[7..0].
$08	**Burst Gate end**	R/W		102	End position of the burst gate. Must be set to burst gate start value + 17. Increments of 1/13.5MHz. 8 bit value = BurstGateend[7..0].
$09	**Video Blanking start 2**	R/W		5	Programmable output pulse intended for video Blanking output for external video DAC. Output is available on Test 0 output. Increments of 1/27MHz. 11 bit value = (VideoBlankingstart2[2..0],VideoBlankingstart1[7..0]).
$0A	**Video Blanking start 1**	R/W		210	
$0B	**Video Blanking end 2**	R/W		5	Programmable output pulse intended for video Blanking output for external video DAC. Output is available on Test 0 output. Increments of 1/27MHz. 11 bit value = (VideoBlankingend2[2..0],VideoBlankingend1[7..0]).
$0C	**Video Blanking end 1**	R/W		210	
					Proc Amp
$20	**Sub Luma Value**	R/W		178	Value subtracted from the processed CVBS output to remove sync. 8 bit value = SubLumaValue[7..0]).
$21	**Luma Gain 2**	R/W		2	Scaling between processed Y output and BT656 Y output. 11 bit value = (LumaGain2[2..0],LumaGain1[7..0]).
$22	**Luma Gain 1**	R/W		80	
$23	**U Gain 2**	R/W		1	Scaling between processed U output and BT656 Cb output. 11 bit value = (LumaGain2[2..0],LumaGain1[7..0]).
$24	**U Gain 1**	R/W		80	
$25	**V Gain 2**	R/W		0	Scaling between processed V output and

Register Offset	Register Name	R/W	Bit Value	Default Value	Description	
$26	**V Gain 1**	R/W		232	BT656 Cr output. 11 bit value = (LumaGain2[2..0],LumaGain1[7..0]).	
Status						
$30	**Status 1**	R			**Status register**	
			7			
			6			
			5			
			4			
			3			
			2			
			1			
			0		PLL inlock = 1	
Control and Status						
$3E	**Control 1**	R/W		0	**Select Test outputs**	
					Test1[2..0] = 111	
					Test1[2..0] = 110	
	Test 1 [2]		5	0	Test1[2..0] = 101	
	Test 1 [1]		4	0	Test1[2..0] = 100	
	Test 1 [0]		3	0	Test1[2..0] = 011	
	Test 0 [2]		2	0	Test1[2..0] = 010	
	Test 0 [1]		1	0	Test1[2..0] = 001	
	Test 0 [0]		0	0	Test1[2..0] = 000	BurstGate
					Test0[2..0] = 111	
					Test0[2..0] = 110	
					Test0[2..0] = 101	
					Test0[2..0] = 100	
					Test0[2..0] = 011	
					Test0[2..0] = 010	
					Test0[2..0] = 001	
					Test0[2..0] = 000	Blanking
$3F	**Control 2**	R/W		0	Do not use Test register.	

Table 5 Register descriptions

Specification

Parameter	Specification	Notes
Standard	NTSC-M	
Frame Rate/Field Rate	30Hz/60Hz	

Table 6 PT3 specification

Measurements

The PT3 NTSC decoder was measured using a Cyclone II development board, (with 2C35 FPGA). The source was the composite output of a Tektronix TG2000 video test generator which was fed through the AD9981 analogue to digital converter of a SingMai DP1 interface board.
The BT656 digital output was converted to component analogue using the ADV7321 digital to analogue converter on the same SingMai DP1 board. The output from the DAC was amplified and filtered using an ADA4412 amplifier and the analogue component measurements were performed on a Tektronix VM700 measurement set.