PT51

‘Universal’ Analogue Video Decoder

User Manual

Revision 1.4
16th November 2018

Revision History

Date	Revisions	Version
07-05-2016	First Draft.	0.1
20-06-2016	Added further video standards. Added NTSC/PAL decoding. AGC description added. Interconnection block diagram added. Modules and some ports renamed. SD demodulation filter added. Anti-aliasing filter for SD added. NTSC/PAL comb filter added.	0.2
05-07-2016	Status registers updated. AFE schematic updated. AGC operation improved. Improved comb filter description. Text corrections.	0.3
12-07-2016	1080i standards added. Schematic port names updated. Text corrections. aCVi description updated.	0.4
10-08-2016	Subcarrier frequencies modified. aCVi description updated. Separate proc-amp controls added for NTSC/PAL/HD standards. Phase comparator filter modified.	0.5
16-08-2016	Verification chapter added.	0.6
29-08-2016	Automatic colour control (ACC) added.	0.7
19-09-2016	Automatic SD/HD format detection added. Changes/additions to the registers. NTSC-960H and PAL-960H standards added. aCVi spectrum (Figure 3) corrected. Manual setting of burst gate positioning added. Manual setting of subcarrier frequency added. Added luma low pass filter (support for HD-CVI and HD-TVI). Sample rate converter added. aCVi 0.5 description added.	0.8
12-10-2016	Text corrections. Control registers modified. Auto cable compensation description updated. Data transfer chapter updated. Measure.v module added. FIFO.v module added. Schematics updated to the SM08 v0.2 revision.	0.9
16-11-2016	Remove FIFO. Remove SRC. aCVi 0.5 removed. DDS clock generator added. Demodulation filter redesigned. AGC register controls added. Anti-aliasing filter added. Data transfer updated.	1.0

Date	Revisions	Version
	Auto cable compensation updated.	
23-11-2016	Add phase detector gain control.	1.1
10-09-2018	DDS clock generator removed. Sample rate converter added. Measure module removed. Control register bits reassigned. Video format control added (Control register 1). Error in register addressing corrected.	1.3
16-11-2018	Document reformatted. Sample rate converter(s) moved to after demodulation and remodulation. Auto format added. Luma low pass filter removed. FIFO added. aCVi1 description removed.	1.4

Contents

Tables

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1. Introduction

PT51 is a video decoder IP (intellectual property) core compatible with the aCVi Advanced Composite Video Interface format and also with NTSC/PAL standards and other analogue HD formats. aCVi is a method to transmit HD video over long distances of coaxial or twisted-pair cable.

The decoder IP accepts digital aCVi/NTSC/PAL/960H encoded video at 10 bit resolution (as well as other non-aCVi HD analogue formats), which it decodes to a 30 bit YCbCr (4:2:2 format) output with separate horizontal and vertical synchronizing pulses and clock. PT51 supports the following HD formats: 720p-25/30/50/60Hz, 1080p-25/30Hz as well as NTSC-M/PAL, NTSC/PAL 960H and NTSC/PAL 1280H video standards.

Control and status registers are written to and read from using a conventional 8 bit wide microprocessor interface.

The intellectual property block is provided as RTL compliant Verilog-2001 source code for FPGAs from all vendors or for ASICs.

Typical resource usage for an Altera FPGA is shown in Table 1 (as compiled for an EP4CE15 FPGA used on the SM08 PT51 evaluation board).

Logic Cells	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers

Table 1 PT51 Altera FPGA resource requirements

An approximate equivalent for ASIC resource usage is ? LCs (logic cell only compile for Altera FPGA) x 14 ~ ?? 2 input NAND gate equivalent. The memory is 26k of single port ROM and the balance is single port RAM.

2. PT51 Module description

The PT51 aCVi decoder IP core comprises 18 Verilog modules in a hierarchical structure (see Table 2).

PT51_decoder.v	Register_control.v	
	AA_Filter.v	
	vid_nco.v	vid.v
		time_nco.v
		rnd_sat.v
	Demod.v	SinCos_ ROM.v
	DemodLPF.v	
	SPG.v	
	Comb_filter	ram_infer_generic.v
	Delay.v	
	Remod.v	
	Procamp.v	
	FIFO.v	ram_infer_generic.v

Table 2 PT51 Verilog file structure.

The top level file is PT51_decoder.v which, in turn, calls 17 of the other modules.

Demod.v calls a third level file SinCos_ROM.v;
vid.nco.v calls vid.v, time_nco.v and rnd_sat.v;
Comb_filter.v calls ram_infer_generic.v;

3. Signal Interconnections

The PT51 signal interconnect diagram is shown in Figure 1.

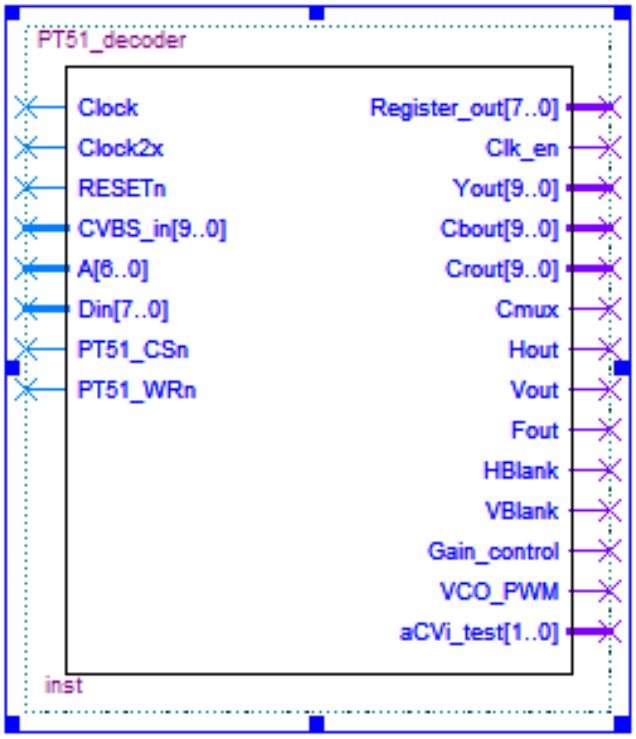

Figure 1 PT51 Block symbol.

The signal descriptions are shown in Table 3, below.

Inputs	
Signal	**Description**
Clock	The clock input from the voltage controlled oscillator (VCO) or fixed clock source. See Table 4 for the required frequency for the various supported formats. Only the rising edge of this clock is used, so the mark space ratio is not critical.
Clock2x	The 2x clock input from the VCO or fixed clock source. See Table 4 for the required frequency for the various supported formats. The rising edge of this clock should be aligned with the rising edge of 'Clock'.
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all registers.
CVBS_in[9:0]	Input digital composite video from ADC. Data should be valid on the rising edge of the sample clock. This input should be straight binary (sync tip bottom ~ code '0', peak video white ~ code '1023').
A[6:0]	Address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT51_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.

PT51_WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers.
Outputs	
Signal	**Description**
Register_out[7..0]	Control output data bus. Outputs the control/status register data selected by the A[6:0] bus.
Clk_en	Clock enable output. All output video and sync signals are valid on the rising edge of Clock when this signal is '1'. This signal is nominally at half the frequency of Clock.
Yout[9:0]	Y (luma) output from the encoder. The output is straight binary, blanking level is 64_{10} and peak level nominally 960_{10}. The data output is valid at the rising edge of 'Clock' when 'Clk_en' is high. Yout[9] is the MSB.
Cbout[9:0]	Cb (B-Y chroma) output from the encoder. The output is offset binary, blanking level is 512_{10}. The data output is valid at the rising edge of 'Clock' when 'Cmux' and 'Clk_en' are high (4:2:2 format). Cbout[9] is the MSB.
Crout[9:0]	Cr (R-Y chroma) output from the encoder. The output is offset binary, blanking level is 512_{10}. The data output is valid at the rising edge of 'Clock' when 'Cmux' and 'Clk_en' are high (4:2:2 format). Crout[9] is the MSB.
Cmux	Data valid output for Cb and Cr outputs. Cb and Cr data is valid on the rising edge of 'Clock' when 'Cmux' is high (4:2:2 data format). 'Cmux' is nominally 37.125MHz for aCVi and 6.75MHz for NTSC/PAL.
Hout	Horizontal sync output from decoder (active low). The falling edge of this output is the 0H timing reference (middle of analogue tri-level sync for HD or falling edge of bi-level sync for SD).
Vout	Vertical sync output from decoder (active low). The falling edge of this output is Line 1 of the field.
Fout	Frame sync output from decoder (low for field 1). Only valid during interlaced video formats.
HBlank	Horizontal blanking output from decoder. The duration of this pulse is the active video period of the standard (e.g. 1280 pixels for 720p standards).
VBlank	Vertical blanking output from decoder.
Gain_control	Pulse width modulated output for the control of the analogue input stage voltage controlled amplifier (AGC). See Chapter 5.
VCO_PWM	Pulse width modulated output for the control of external voltage controlled oscillator frequency (VCO control voltage). See chapter 6.

Table 3 PT51 Input/Output signals

The Verilog instantiation of PT51 is shown below:

```
// Instantiate aCVi decoder (PT51)

PT51_decoder PT51_decoder_inst
(
.Clock(Clock_sig) ,                    // input  Clock_sig
.Clock2x(Clock2x_sig) ,                // input  Clock2x_sig
.RESETn(RESETn_sig) ,                  // input  RESETn_sig
.CVBS_in(CVBS_in_sig) ,                // input [9:0] CVBS_in_sig
.A(A_sig) ,                            // input [6:0] A_sig
```

```
.Din(Din_sig) ,                    // input [7:0] Din_sig
.PT51_CSn(PT51_CSn_sig) ,          // input  PT51_CSn_sig
.PT51_WRn(PT51_WRn_sig) ,          // input  PT51_WRn_sig

.Register_out(Register_out_sig) ,  // output [7:0] Register_out_sig
.Clk_en(Clk_en_sig) ,              // output  Clk_en_sig
.Yout(Yout_sig) ,                  // output [9:0] Yout_sig
.Cbout(Cbout_sig) ,                // output [9:0] Cbout_sig
.Crout(Crout_sig) ,                // output [9:0] Crout_sig
.Cmux(Cmux_sig) ,                  // output  Cmux_sig
.Hout(Hout_sig) ,                  // output  Hout_sig
.Vout(Vout_sig) ,                  // output  Vout_sig
.Fout(Fout_sig) ,                  // output  Fout_sig
.HBlank(HBlank_sig) ,              // output  HBlank_sig
.VBlank(VBlank_sig) ,              // output  VBlank_sig
.Gain_control(Gain_control_sig) ,  // output  Gain_control_sig
.VCO_PWM(VCO_PWM_sig) ,            // output  VCO_PWM_sig
.aCVi_test(aCVi_test_sig)          // output [1:0] aCVi_test_sig
);
```

Figure 2 shows the interconnections between the PT51 IP core and the voltage controlled oscillator (if used) and analogue front end/ADC. The analogue front end/ADC requirements are discussed in detail in chapter 5 and the clock requirements in chapter 6.

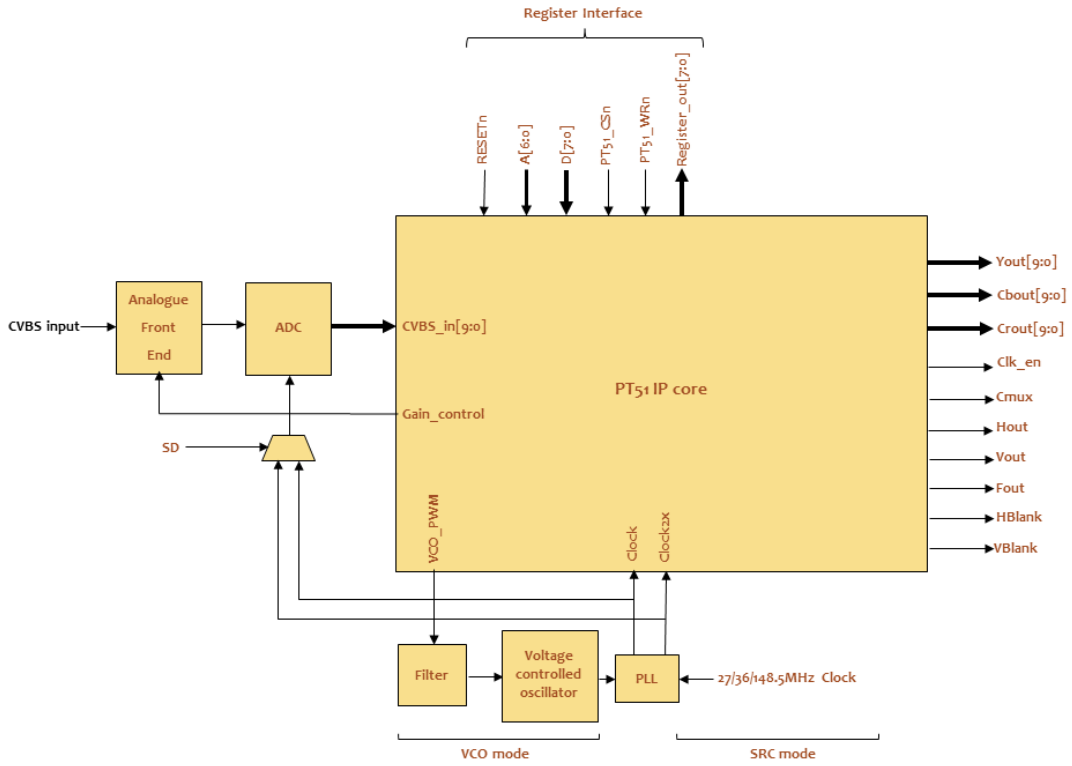

Figure 2 PT51 IP core interconnections.

4. aCVi Overview

TBD.

5. Analogue Front End

Figure 6 shows the analogue front end (AFE) for the PT51 evaluation board (SM08). The board can accept either twisted pair differential inputs (J1) or single ended coaxial inputs (J2). For the latter, the coaxial input has a pseudo-differential input, giving some degree of low frequency noise rejection (e.g. hum).

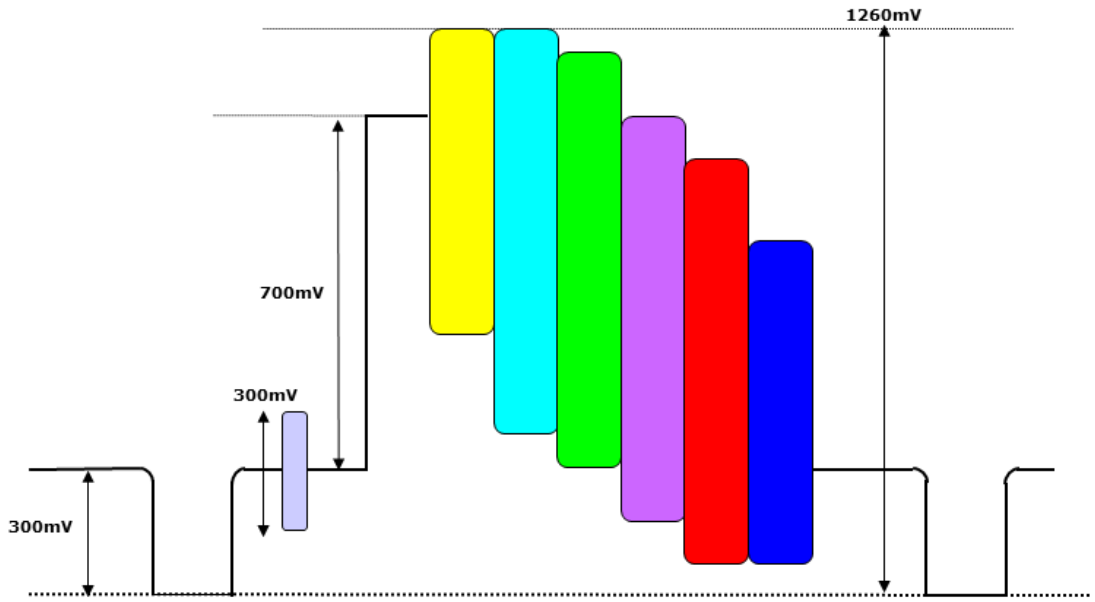

Figure 3 aCVi input levels

The typical input voltage levels (for a 100% colour bar input) are shown in Figure 3. The sync, luma and colour modulation depth for the other HD analogue formats are similar to NTSC/PAL which permits a common front-end design to be utilized. The analogue front end is designed to accommodate a +3dB overhead on this signal to allow over-range inputs without clipping.

U9 and U15 convert the (pseudo) differential inputs to a single ended output with a gain of x1 (U8 compensates for the 6dB attention through U15). U10 is a programmable gain amplifier that is controlled by the PWM input signal, 'Gain_control', which in turn is controlled by register $04 of the PT51 (manual gain) or by the automatic gain control (AGC) loop. The VGA loop is shown in Figure 4.

The digital CVBS signal is low pass filtered in the SPG module to remove high frequency noise and chroma and the most negative video value (negative sync tip) and the back porch value are measured to give the sync pulse amplitude. The measured sync amplitude is compared with a reference value (the 0dB sync amplitude) to produce a correction gain value. The filtering of the sync amplitude measurement, and the external analogue low pass filter, set the response time of the AGC loop. The gain response curve of the AD8337 is shown in Figure 5.

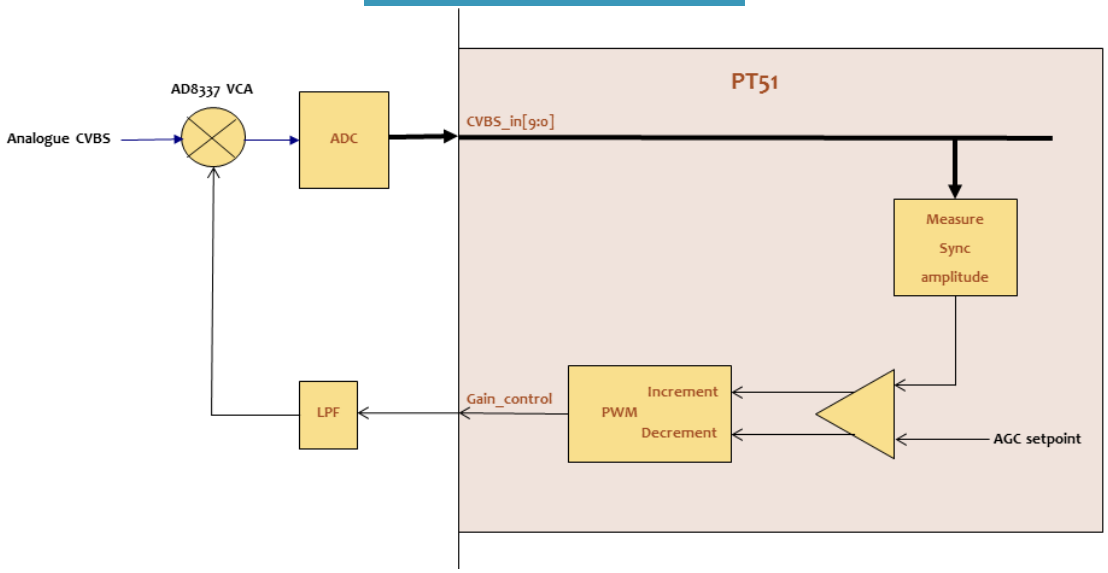

Figure 4 AGC Control loop.

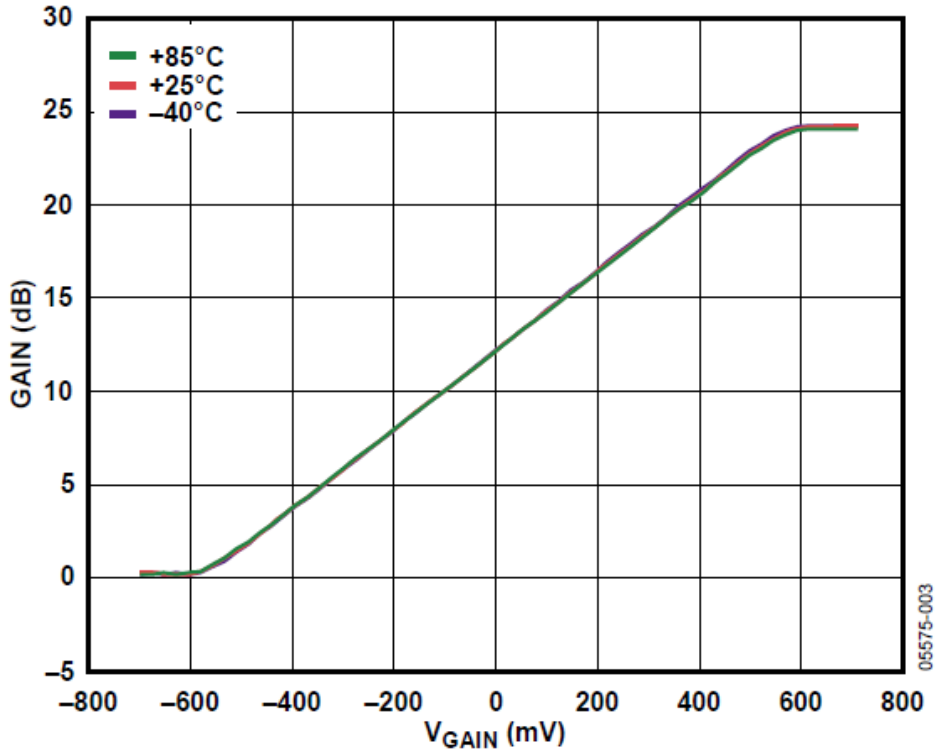

Figure 5 AD8337 PGA gain response.

The gain correction is then converted to a PWM signal, which is low pass filtered externally to the PT51 (by R41 and C50) to convert it to an analogue control voltage. The AD8337 provides a +18dB control range. Note that the AGC relies on the maintaining of the correct sync to video ratio (3/7) and if this ratio is not maintained the video may not be compensated for correctly or may clip.

The output of the PGA is then clamped to ensure the video signal is scaled through the ADC correctly under large variations in average picture level (APL). The bottom reference of the ADC is used to clamp the most negative part of the input signal, using an ideal diode formed by D5 and U11-B. The black level restoration is performed digitally in the PT51 decoder.

The clamped video is then digitized in a 10 bit ADC, U19, an AD9215, which is clocked at 74.25/148.5MHz for HD video formats, 54MHz for NTSC/PAL and 72MHz/90MHz for NTSC/PAL 960H/1280H standards (see Figure 7). The output from the ADC is straight binary coded 10-bit digital CVBS video.

To ease the requirements of an analogue anti-aliasing filter for NTSC/PAL operation, the ADC is over-sampled at 54MHz/72MHz/90MHz. The PT51 low pass filters this in an anti-aliasing filter to remove out of band components and allowing the video input to be decimated to half of this sample rate. The anti-aliasing filter is bypassed in HD modes.

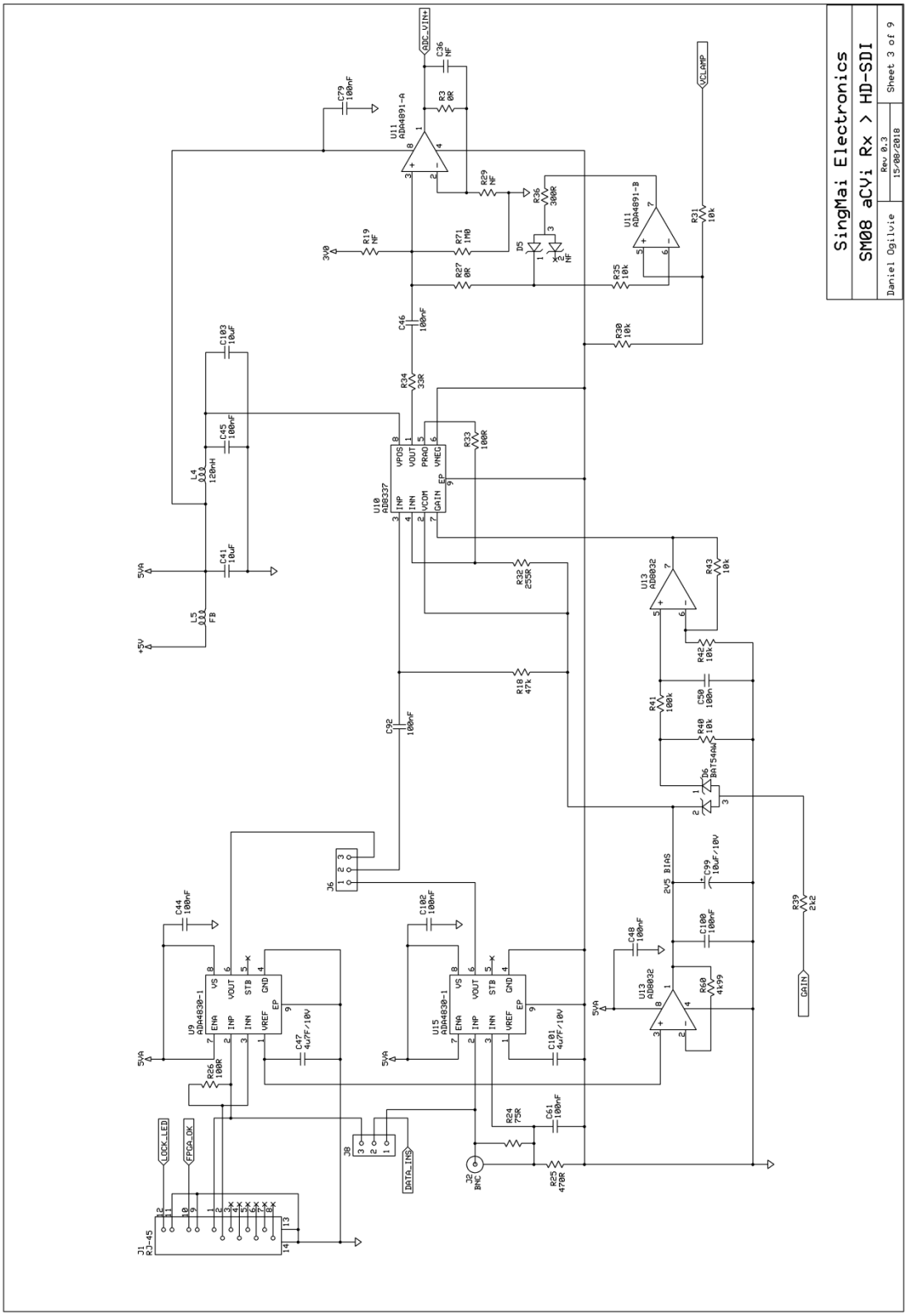

Figure 6 Analogue Front End schematics.

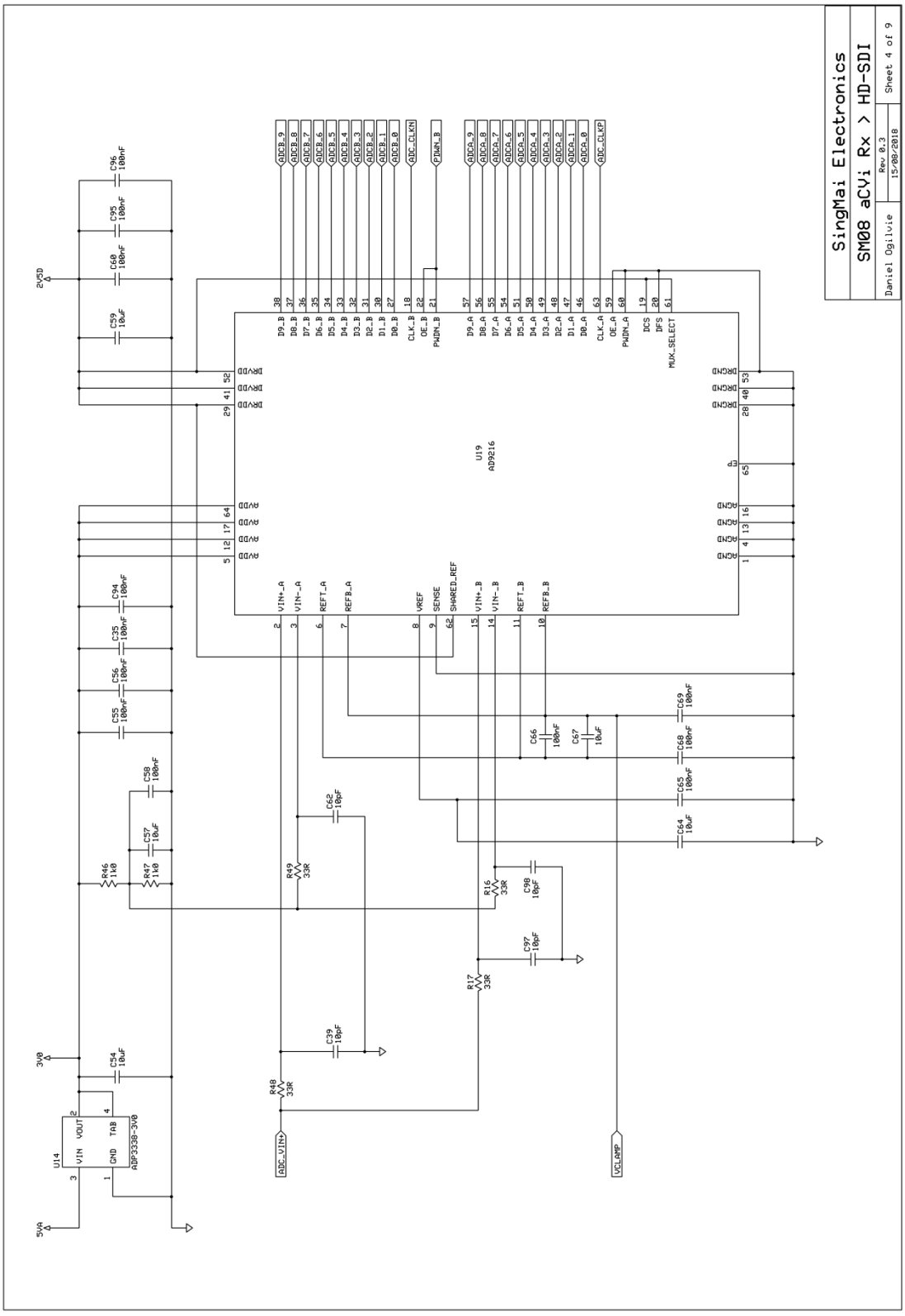

Figure 7 ADC schematics.

For an ASIC application an example input schematic is shown in Figure 8.

The CVBS input is terminated in 75Ω and AC coupled into the video input of the ASIC (C1) indicated by the dotted line on the schematic. R1 and C2 form a simple low pass filter to remove aliasing components. The low pass filter requirement is relaxed by over-sampling the ADC at 54MHz/72MHz/90MHz.

The ASIC input should be biased to mid-rail and present a high impedance (>10kΩ) input impedance over the required video frequency range.

The output of the buffer amplifier is then DC restored, such that the bottom sync tip is clamped to the bottom reference of the ADC (i.e. the most negative value of the CVBS input results in digital code '0' from the ADC).
The clamped video is then buffered and converted to a differential input for driving the ADC. The output of the ADC then provides the CVBS[9:0] (10-bit) input to the PT51.

The peak-to-peak video input range for a 100% modulated PAL colour bar signal is 1.26V. It is prudent to accommodate over-range inputs without clipping so a 2-3dB overhead should be designed for (i.e. 1.26V +3dB = 2.26V): the AFE input stage supply voltage should therefore be >2.5V.

The performance of the complete front end should present no limit to the performance of the PT51. Typically for PAL, the differential gain and phase should <1% and <1°, respectively; the bandwidth should be 5.75MHz ± 0.15dB and the group delay should be <15ns (ideally <10ns). RMS noise from 0 - 5.75MHz should be <-60dB.

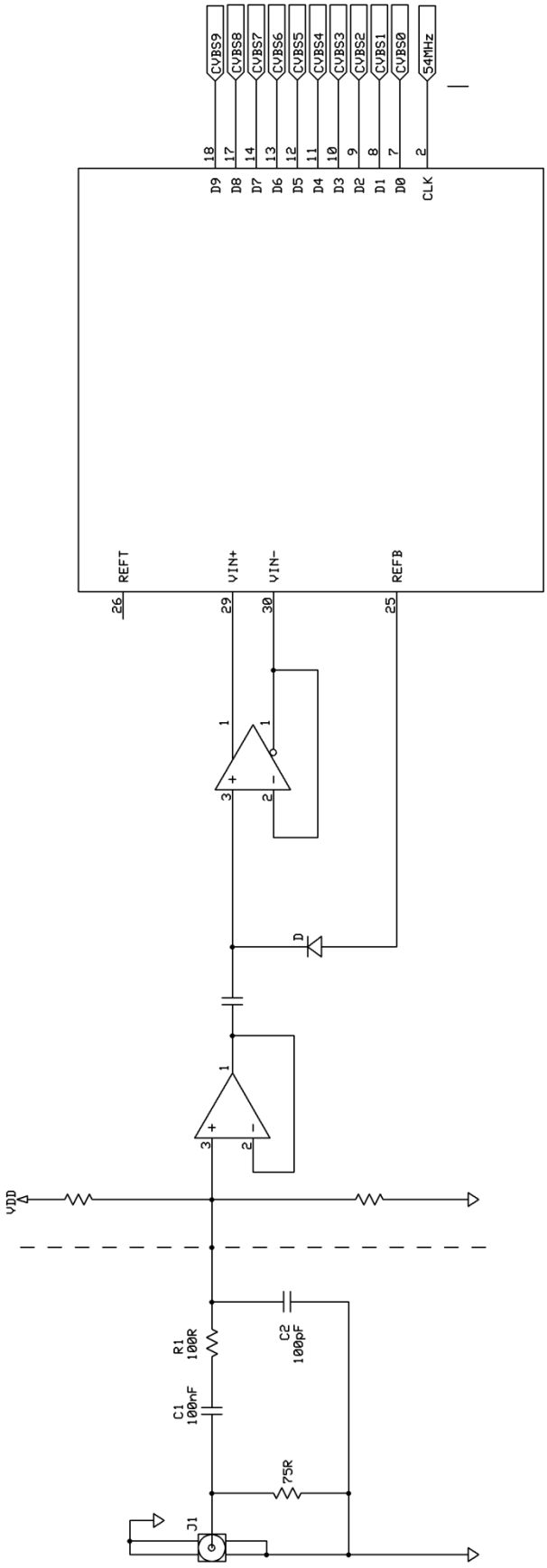

Figure 8 AFE ASIC application schematic.

6. Synchronisation modes

The PT51 needs to produce a line locked output – that is to say, a video output pixel must appear at the same point in time relative to the horizontal sync pulse. Failure to do so will mean vertical edges will be jagged.

The clock rates for the supported video standards are shown in Table 4.

Clock	NTSC/PAL	960H	1280H	AHD	HD-CVI	HD-TVI
ADC clock	54MHz	72MHz	90MHz	148.5MHz	74.25/148.5[1]	148.5MHz
PT51 Clock	27MHz	36MHz	45MHz	148.5MHz	74.25/148.5[1]	148.5MHz
PT51 Clock2x	54MHz	72MHz	90MHz	NR[2]	NR[2]	NR[2]

Table 4 PT51 and ADC sample rates.

[1] Clock frequency = 74.25MHz for 720p-25/30Hz and 148.5MHz for 1080p-25/30Hz.
[2] This clock is not required.

The PT51 provides two methods to produce a line-locked output:

1. The PT51 provides a VCO_PWM output which can be filtered to produce an analogue control voltage to control the frequency of a voltage-controlled oscillator (VCO). This VCO output provides the clock for PT51.
2. The PT51 accepts a fixed clock input frequency and uses sample rate converters and sample dropping to align the video with the clock edge and ensure there are the correct number of samples per horizontal line. A FIFO retimes the output to ensure there is a continuous output without missing samples.

The PT51 SPG module extracts the horizontal sync signals from the composite CVBS inputs. The SPG module also divides the 'Clock' input to produce a signal at the same approximate frequency as the horizontal line pulse. For example, for 720p/60Hz, dividing the 74.25MHz clock by 1650 (the number of pixels/line according to the video standard) produces 45kHz, the line frequency of the 720p/60Hz standard. The SPG module then compares the phase of this 45kHz signal and the recovered horizontal sync signal. The error in phase is then used to adjust the frequency of the 'Clock' input such that the two falling edges of the signals align. When this occurs the horizontal input sync and the Clock will be in phase and we will have a line-locked output.

In synchronizing mode 1 (VCO mode) the phase error word generated in the SPG module is converted to a pulse width modulated (PWM) which is converted to analogue voltage to control the frequency of the VCO. The external VCO circuit used in the PT51 evaluation board (SM08) is shown in figure 9.

The PWM signal is low pass filtered (R11 and C32) and buffered (U7), to become the analogue control voltage to a VCXO (voltage controlled crystal oscillator). The frequency output of this oscillator should comply with the requirements shown in Table 4. In addition, for SD standards (the anti-aliasing filter and the line delays for the comb filter require it), a twice clock frequency input to the PT51 is required (Clock2x). The rising edges of Clock and Clock2x should be aligned.

In lock mode 1, the sample rate converters are set to bypass by setting Control register 3, bit 6 to '1'. The SRC will then produce a fixed half frequency clock enable output that is used to gate all subsequent registers. For example for NTSC/PAL, the video and input clock to the sample rate converter (SRC) is 27MHz (the ADC output at 54MHz has been decimated by a factor of two in the anti-aliasing filter module). All subsequent registers are also clocked at 27MHz, but enabled using the Clk_en output of the SRC, which is at 13.5MHz. Effectively the PT51 is running at 13.5MHz.

A VCXO (Voltage Controlled Crystal Oscillator) is used on the SM08 PT51 evaluation board. However any oscillator may be used that meets the stability requirement. The 'pull' range of VCXO is limited,

which means that some out-of-range NTSC/PAL inputs cannot be locked to because we cannot adjust the frequency of the VCXO more than ±150ppm (±0.15%). To accommodate all NTSC/PAL signal sources, including mechanically scanned sources such as VCR or laserdisc, a pull range of ±7% should be designed for.

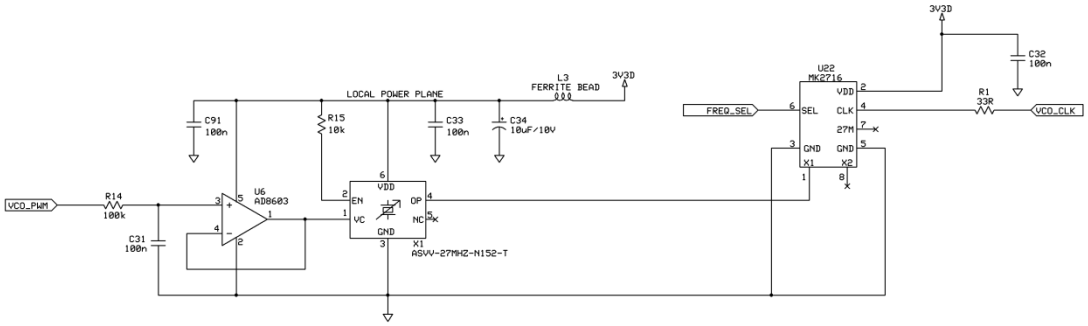

Figure 9 External VCO schematic.

For the comb filter to separate the chroma and luma properly, and to reduce the jitter on the chroma vectors to less than 1° (the broadcast NTSC/PAL specification), the clock jitter should be less than 1/(4.4335MHz [PAL subcarrier frequency] x 360) = 626ps. This is the short term jitter, which for the comb filter requirement is 2/15.625kHz = 128µs (the aperture of the PAL comb filter is 2 horizontal lines/field): i.e. the short term (128µs) peak jitter of the VCO should be <0.6ns.

In lock mode 2, the PT51 only requires a fixed clock input. If both lock modes are required Control, register 3, bits 5:4 can be set to '11' which sets a 50% duty cycle output to the VCO_PWM output to adjust the VCO to its mid-point frequency range.
The horizontal phase error is generated in the same way as for lock mode 1. However, the phase error word is instead used to adjust the phase of the video input instead of the clock. This is achieved by using a Farrow filter structure in the SRC. The SRC can be thought of as a multi-phase filter which, by selected appropriate taps allow us the alter the phase of the output video over a ±0.5 pixel range. If the input video is more than ±0.5 pixels in error from our generated horizontal clock, then the Clk-en (clock enable) can add or subtract cycles of the clock to effectively produce a coarse phase adjustment. Under this condition the video output may not be continuous.

Figure 10, upper, shows the continuous output video when in lock mode 1. In this mode we adjust the frequency the clock, so although the 13.5MHz nominal output may be slightly more or less than this, the video output is continuous.
In lock mode 2, the Clk_en output may not be at a fixed half frequency and the output may produce two cycles of video data at 27MHz, or no new video data for a clock period (see the bottom waveforms of Figure 10). To avoid this non-continuous output a FIFO is used to re-time the output.

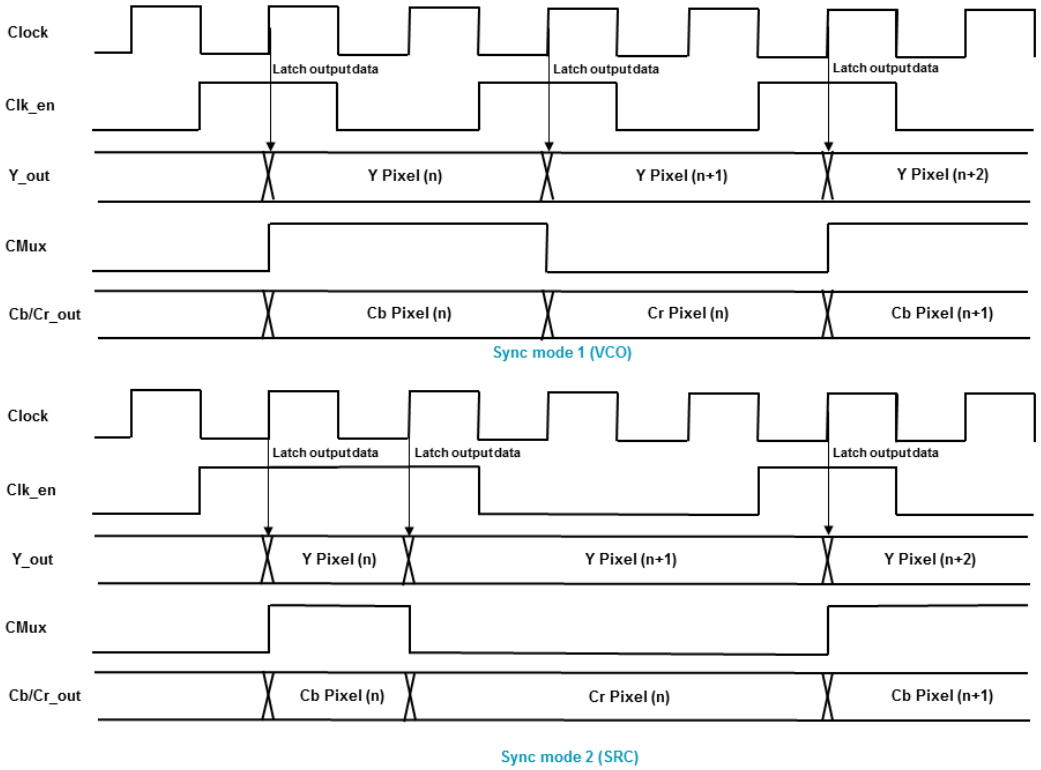

Figure 10 PT51 lock modes: Output Timing.

7. Technical Overview

A simplified block diagram of the front end of the PT51 decoder is shown in Figure 11.

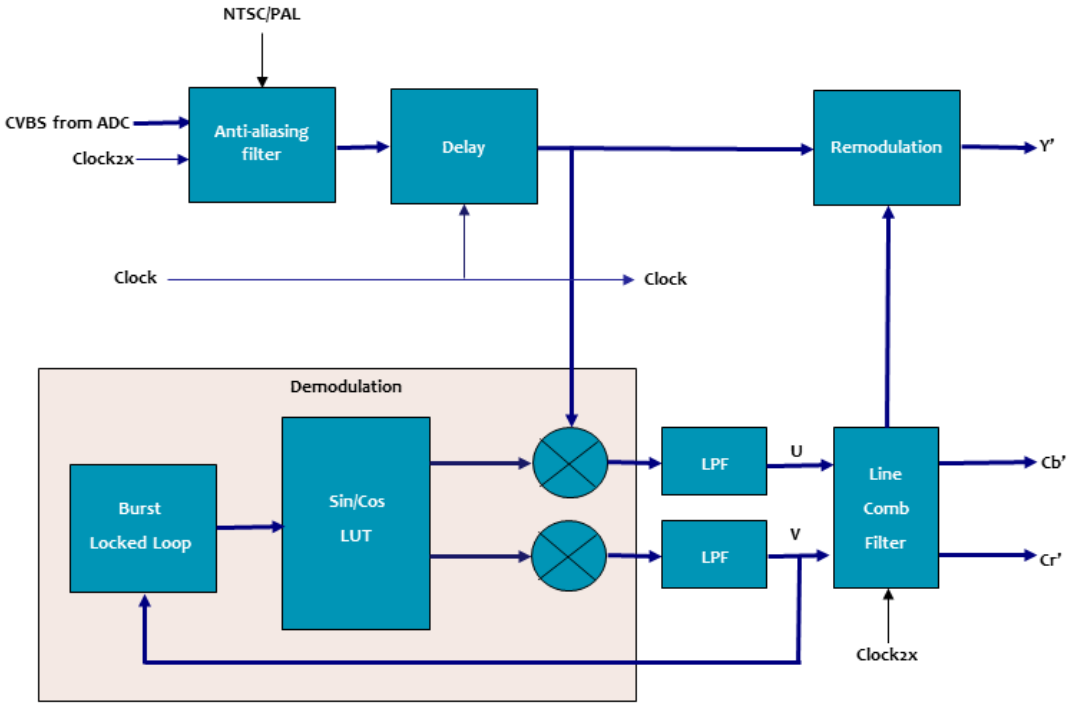

Figure 11 PT51 Block diagram - Front end.

The aCVi input from the ADC is straight binary coded at 10-bit resolution. The sample rates for the ADC and PT51 decoder are summarized in Table 4.

Analogue clamping prior to the ADC ensures the most negative value of the input signal (the sync tips) are clamped to the negative reference of the ADC (code value '0').

The following is a brief description of each Verilog module.

7.1 PT51_decoder.v

This is the top level module for the PT51. It provides the interconnection between all the other modules.

7.2 Register_control.v

A conventional 8 bit microprocessor style control is used to write and read to the PT51 control registers. Details of the interface may be found in Chapter 8 and the register descriptions may be found in Chapter 9.

7.3 AA_Filter.v

The SD video inputs are over-sampled (at 54MHz, 72MHz or 90MHz) to ease the requirements of any analogue anti-aliasing filter. For SD operation therefore, the ADC input is low pass filtered so it may be decimated to a 27MHz/36MHz/45MHz sampling rate. The response of this filter for NTSC/PAL is shown in Figure 12. For HD operation, this filter is bypassed.

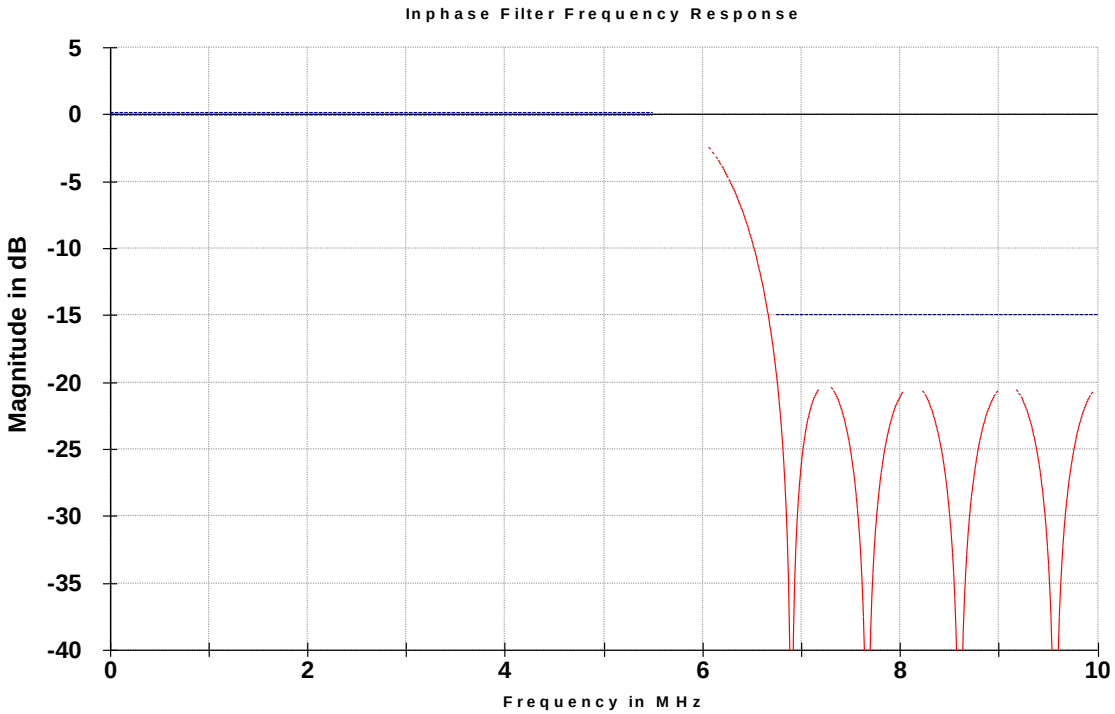

Figure 12 Anti-aliasing filter.

7.4 Demod.v

A free-running subcarrier frequency is generated using a 32 bit ratio counter clocked from the input clock.

$$ratio = \frac{\text{phase change per line}}{\text{pixels per line}} = \frac{F_{sc}}{\text{Clock frequency}} = \frac{\Delta\theta_{sc}}{360^\circ} = \frac{\text{subcarrier seed}}{2^{32}}$$

The top 11 bits of this ratio counter (the phase word) are used by the demodulator to generate the sine and cosine waveforms.

For the demodulation to correctly operate the generated subcarrier must be frequency and phase locked to the CVBS video subcarrier which is done by measuring the amplitude of the demodulated and low pass filtered V output during the colour burst. If the frequency and phase of the free-running subcarrier and the colour burst are the same then this error will be zero. The reference for the BLO is the demodulated and filtered V output from the demodulator low pass filter; 32 samples of this waveform are taken during the burst pulse (16 for NTSC/PAL); the burst gate pulse from the SPG is used for this purpose.

The seed word is modified using the phase error signal until the input colour burst and the ratio counter are phase locked.

The lower 9 bits of the 11-bit phase output from the BLO (burst locked oscillator) are used to address a sine and cosine lookup table (SinCos.v). These 9 bits comprise the phase angle, at subcarrier frequency, within a single quadrant and the top two bits are the quadrant – this method saves memory by only requiring a single quadrant of sin and cos values to be stored in the LUT. The output of the Sin/Cos LUT is a 24 bit word; 12 bits cosine and 12 bits sine. The quadrant signs are used to manipulate the sine and cosine data such as to construct a full waveform.

The reconstructed sine and cosine waveforms are then multiplied by the input CVBS composite video from the ADC. The output of the sine channel is the demodulated U signal and the cosine channel is the demodulated V output. One over-range bit allows for twice subcarrier frequency components (removed by the subsequent low pass filter).

7.5 DemodLPF.v

The output of the demodulator also comprises twice subcarrier frequencies. The output is therefore low pass filtered using a 47-tap filter, the response for which is shown in Figure 13 (for NTSC/PAL standards).

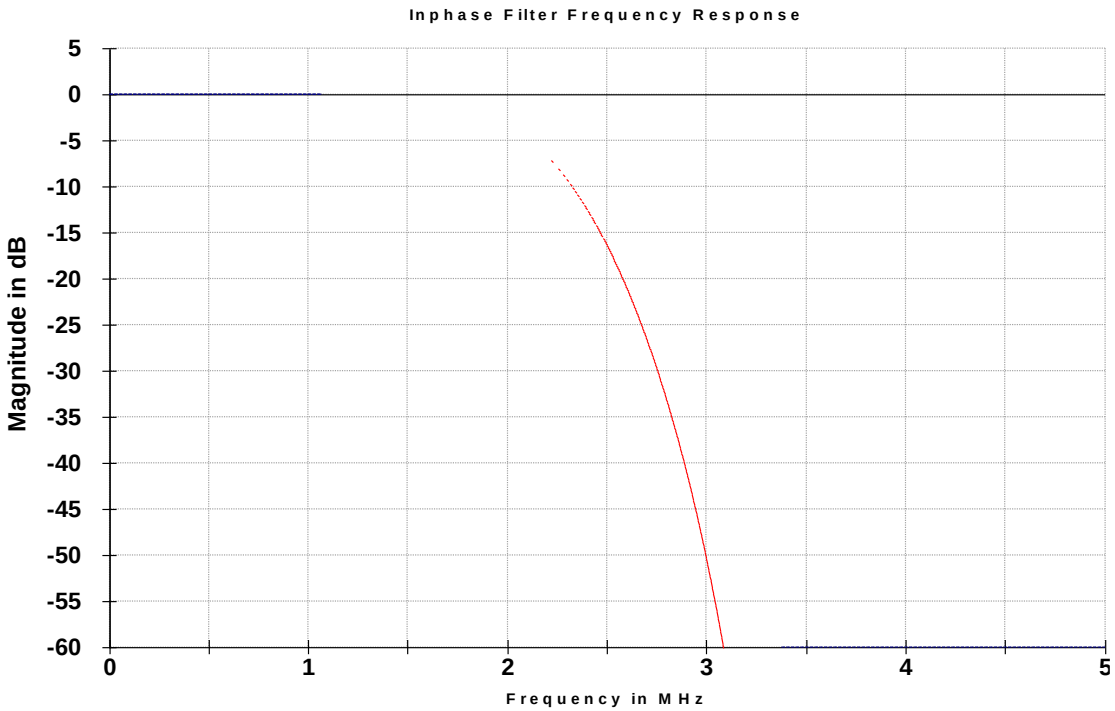

Figure 13 Chroma demodulator low pass filter (NTSC/PAL).

7.6 Delay.v

The CVBS, Sin and Cos waveforms are passed through a compensating delay (to compensate for the demodulation and demodulation low pass filters).

7.7 Comb_filter.v

Because the higher luma frequencies and the modulated chroma frequencies overlap (for NTSC/PAL) a line comb filter is used to separate them. This is possible because the chroma subcarrier has a fixed phase relationship with respect to the horizontal line frequency whereas the high frequency luma does not. For example, for NTSC, the subcarrier frequency is 227.5 times the horizontal frequency, meaning there is a 180° phase shift in the subcarrier for every line of a field.

The low pass filtered U and V video are delayed in two line delay memories. For NTSC the current and the two delayed components are added together in a 1/4*0H + 1/2*1H + 1/4*2H filter. For PAL the comb filter is (1/4*0HU + 1/2*1HU + 1/4*2HU) + [(0HV – 2HV) * PALswitch] and (1/4*0HV + 1/2*1HV + 1/4*2HV) + [(0HU – 2HU) * PALswitch] where the PAL switch contribution is crosstalk cancellation and allows the PAL comb to have the same 2 line aperture as NTSC (because of the additional 90° colour burst switch in PAL, usually a 4 line comb is required).

For the comb filters to operate correctly the phase relationship of the colour component must be maintained; if not the HF luma will not be cancelled and can even be reinforced. It is therefore necessary to detect when the comb filter fails and switch to a better mode. The decision on the comb mode is made on a pixel by pixel basis using the amplitude differences of the Y, U and V components across the line comb filter aperture. Because the Y input still has chroma on it, it is low pass filtered in a 15 tap FIR filter, whose response is shown in Figure 17.

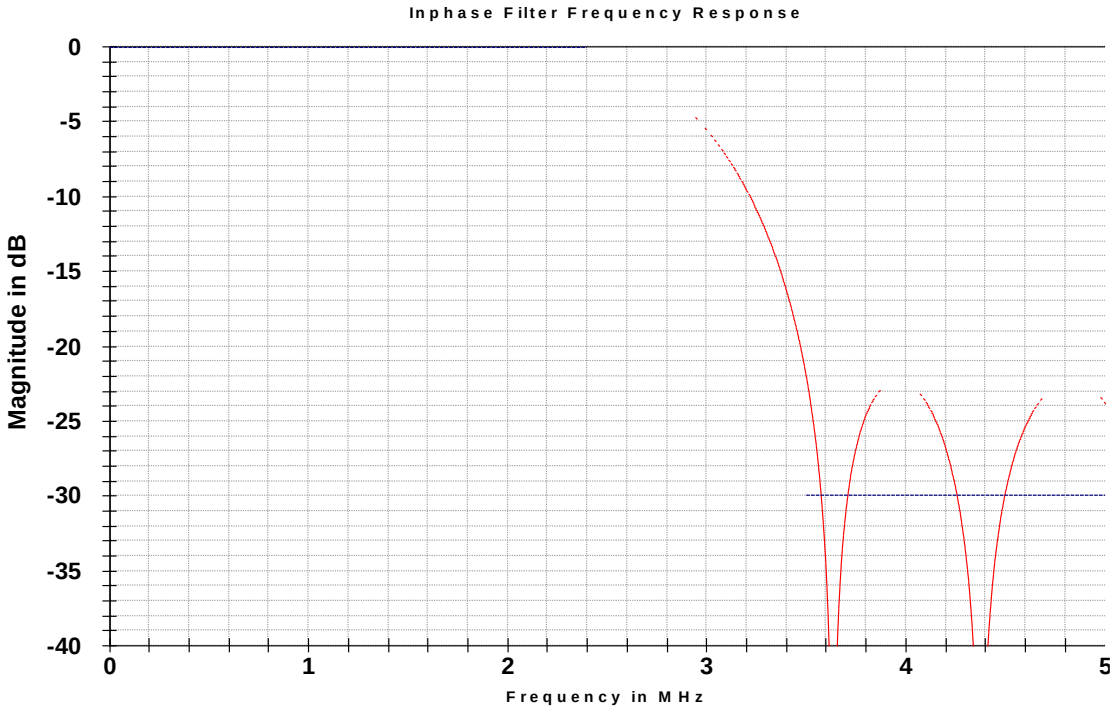

Figure 14 Comb filter luma LPF.

In SD video mode, if the comb filter fails, a large portion of the luma signal (subcarrier frequency ± the demodulation filter response) is removed which gives very 'soft' images with high levels of cross-colour. To alleviate this the chroma signal is low pass filtered using a ¼, 0, 0, 0, ½, 0, 0, 0, ¼ low pass filter (13.5MHz sampling).

The comb mode (line comb or notch mode) can be forced using control register 2 and also, the comb mode selected in adaptive mode may be viewed. The comb filter is bypassed for formats where the luma and chroma are non-overlapping.
Note, to reduce the memory size for the line delays and because the chroma has been shifted to baseband, the comb filter is effectively clocked at half clock frequency.

7.8 Remod.v

The combed U and V components are then frequency shifted back to the subcarrier frequency using the delayed sine and cosine waveforms from the Demod.v module, added together to create a chroma component (which in line comb module will contain no high frequency luma information) and subtracted from the composite video to form a 'clean' luma signal. The complementary nature of this architecture ensures there is no missing information from the final luma output.

The block diagram of the back end of the PT51 is shown in Figure 18.

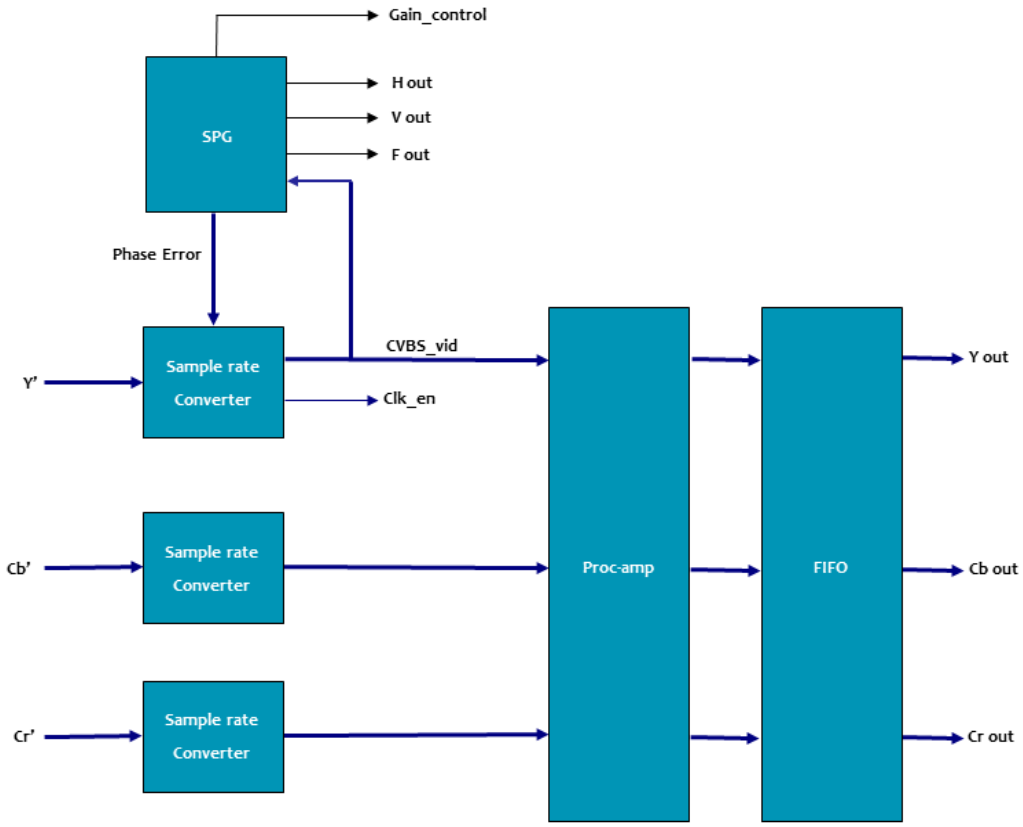

Figure 15 PT51 Block diagram - Back end.

7.9 SPG.v

A fixed offset is subtracted from the CVBS video such that the midpoint of the sync pulse is at value 0. The horizontal counter addresses a look up table whose output coefficients form an FIR low pass filter to remove chroma composite video. The coefficients are multiplied by the offset video and accumulated across the aperture of the filter, being updated once per horizontal line. The frequency response of the sync filter for HD standards is shown in Figure 19 and for SD standards is shown in Figure 20.

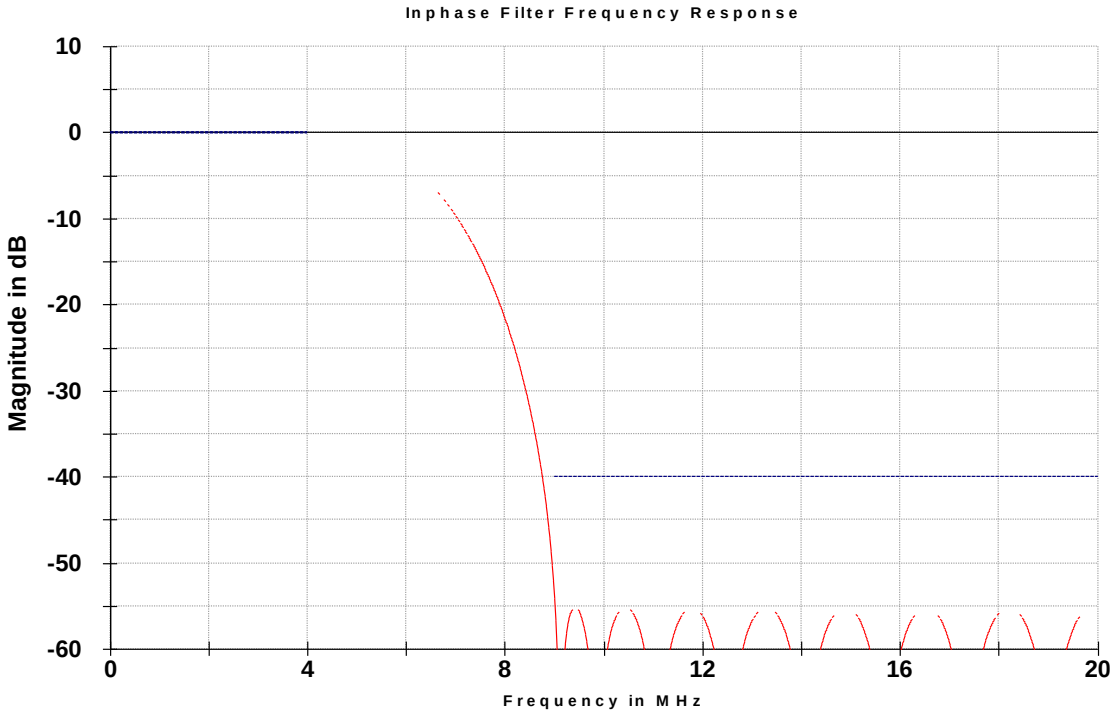

Figure 16 Phase detector low pass filter response (HD standards).

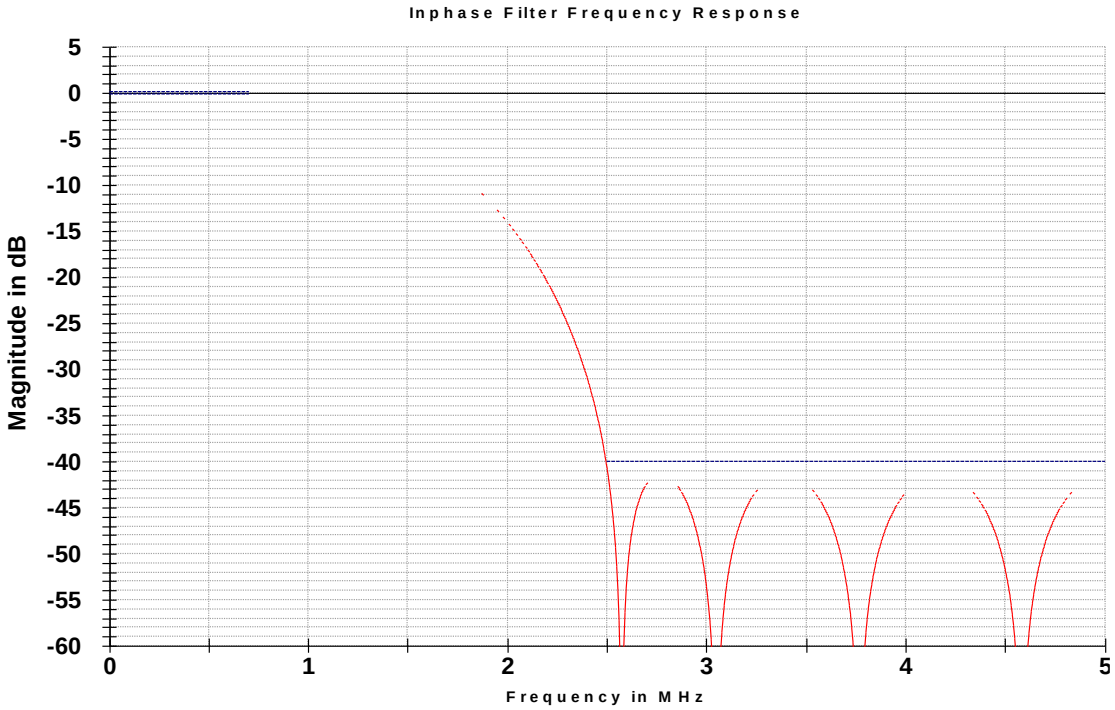

Figure 17 Phase detector low pass filter response (SD standards).

When the midpoint of the falling edge of the horizontal pulse is coincident with the centre tap of the FIR filter the accumulated result will be zero. When they are not coincident an error will be generated. This error is filtered using a recursive filter (integrator) and proportional and integral terms are added to create an error word which is converted to a PWM signal to control an external voltage-controlled oscillator (VCO).

The horizontal pixel counter is used by the SPG, (sync pulse generator), to provide the horizontal timing pulses required by the decoder, including the burst gate pulse for the demodulator, which must lie in the centre of the colour burst signal.

The vertical field pulses are recovered by using a digital integrator on the sliced filtered video. The SPG also provides Vout (vertical field), Fout (frame ID for interlaced video) and Hout (horizontal) synchronizing pulses.

The SPG also detects the input video standard. The number of field pulses/second, the number of lines/field, whether interlace is detected and the number of pixels/line are all used to determine the input standard. The resulting default values for each standard are then automatically loaded into the appropriate registers (in auto-register mode).

7.10 Vid_nco.v

The comb filtered U and V (in SD mode) or low pass filtered U and V (in HD mode) together with the Y output of the remodulator are sample rate converted (in lock mode 2 – in lock mode 1 the sample rate converter is bypassed [Control Register 3, bit 6]).

Vid_nco.v and its three sub-modules, time_nco.v, vid.v and rnd_sat.v form a video sample rate converter. Three implementations of the sample rate converter are used for the three Y, U and V channels.

In lock mode [2] the front end is running at a fixed 27MHz clock rate. The sample rate converter clocks a ratio counter at 27MHz and provides a 13.5MHz (average) enable output used to gate the back end clock of the decoder. The ratio counter is adjusted by adding/subtracting a phase error signal – generated by the horizontal phase detector in the SPG.v module – to the seed value.
The ratio counter also provides a phase word which is used to interpolate the 'mid-point' of the video samples and map the incoming video onto the new clock domain. The video interpolator can adjust the video by ±0.5 pixels – more adjustment is provided by dropping or adding clock cycles via the enable signal.

The interpolator uses a Farrow structure; the output from the sample rate converter is an approximate 13.5MHz enable signal (Clk_en) and the interpolated composite video.

7.11 Procamp.v

The outputs of the sample rate converters are conditioned by the processing amplifier. First the black level offset of the luma (measured in the SPG module) is subtracted from the luma signal to set the black level at zero. The luma is then offset (to 64 code) and amplified to provide a 960 code (10 bit) output for a 75/100% colour bar input.

The low pass filtered chroma outputs are amplified separately to provide a nominal $\pm 262.5_{10}$ code output for a 75% colour bar input. The Cb and Cr outputs are offset binary, with the blanking level at 512_{10}.

7.12 FIFO

Figure 10 shows that the output of the Proc amp module, in lock mode 2, may now provide continuous samples at the effective clock rate of half-clock. This may not be issue when writing into

memory, but it will be an issue if interfacing to a device such as an HDMI or HD-SDI transmitter where it is expected to have valid video on each edge of the clock.

To remedy this problem the video is retimed using a FIFO. The YUV video is written into the FIFO using the clock and the Clk_en enable signals and read out using the clock and a free-running half clock signal, thereby ensuring video is valid on each edge of the clock.

8. Register interface

Figure 22 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via a 7 bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT51_CSn (chip select) input must be asserted low and the A[6:0] register address and the data for this register set up. The PT51_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT51_CSn input should then be returned high.

For the write to occur reliably the address (A[6:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT51_WRn pulse.

The address input also selects the register data that is presented on the Register_out[7:0] bus. This output is independent of the PT51_CSn or PT51_WRn inputs.

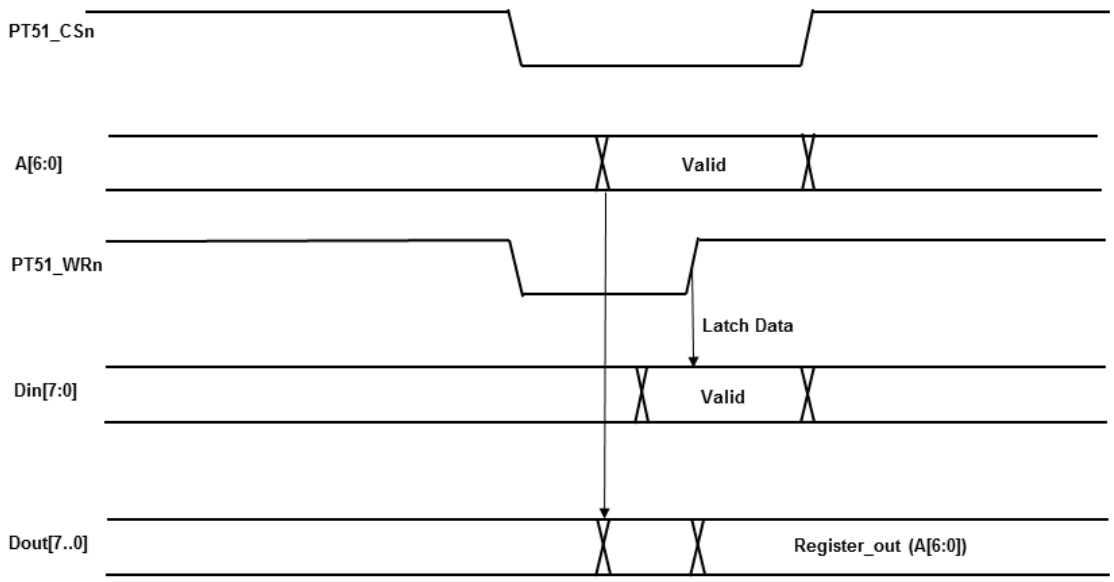

Figure 18 PT51 Register timing.

9. Register descriptions

Table 5 lists all of the control and status registers. All of the registers are 8 bit; unused register bits read back as zeros.

Please note that some registers can be set to values that are illegal and will produce invalid outputs.

Asserting the RESETn input resets the PT51 registers to their default values.

Register Offset	Register Name	R/W	Bit Value	Description
Control Registers				
$00	**Control_1**	R/W		
	Auto standard		7	If reset to '0' the video standard is preset manually using bits 3:0. If set to '1' (default value) the detected video standard is determined automatically.
	Video format		6:4	Manually sets the video format ('111' not used) if Control register 2 bit 6 is set to '0'.
	Video standard		Bits 6:4	000 / 001 / 010 / 011 / 100 / 101 / 110
				SD / 960H / 1280H / aCVi-2 / AHD / HD-CVI / HD-TVI
			Bits 3:0	
			0000	**NTSC / NTSC / NTSC / / 720p/25 / 720p/25 / 720p/25**
			0001	**PAL / PAL / PAL / / 720p/30 / 720p/30 / 720p/30**
			0010	**720p/50 / / 720p/50**
			0100	**720p/60 / / 720p/60**
			0110	**1080p/25 / 1080p/25 / 1080p/25**
			1000	**1080p/30 / 1080p/30 / 1080p/30**
$01	**Control_2**	R/W		
	Auto register		7	If set to '1' (default value) the parameter values are set to their default values depending on the video standard (note: only those standards listed in bits [3:0] have default values assigned). If set to '0', Registers $20-$4F may be programmed manually.
	Auto Format		6	If set to '1' the HD video format is determined automatically (e.g. AHD, HD-CVI etc.). If set to '0' Control Register 1 bits 6:4 determine the video format.
	View comb mode		5	In SD mode only (Control 1 bits 6:4 = '000'), if set to '1' this bit enables the auto comb mode selection to be displayed. If set to '0' the video output is shown.
	Auto comb mode		4	In SD mode only (Control 1 bits 6:4 = '000'), if set to '1', the comb mode is set automatically depending on the comb failure detection logic. If set to '0' the comb mode is manually set using the manual comb mode bits [3:0].
	Manual comb mode (Luma)		3:2	Bit 1 / Bit 0 / If the auto comb mode is set to '0'.
				0 / 0 / Forces low pass mode.
				0 / 1 / Forces line comb mode
				1 / 0 / Bypasses line comb
				1 / 1 / Not defined
	Manual comb mode (UV)		1:0	Bit 1 / Bit 0 / If the auto comb mode is set to '0'.
				0 / 0 / Forces low pass mode.
				0 / 1 / Forces line comb mode
				1 / 0 / Bypasses line comb
				1 / 1 / Not defined
$02	**Control_3**	R/W	7	Not used.
			6	Bypasses the sample rate converter if set to '1'. If set to '0' the sample rate converter operates, and the input clock should be a fixed frequency.
			5:4	Bits [5:4] / VCO_PWM output
				00 / Error output (VCO lock mode)
				01 / Force VCO_PWM output to '0'.
				10 / Force VCO_PWM output to '1'.
				11 / Force VCO_PWM output to 50% (SRC mode when using a VCO for

Register Offset	Register Name	R/W	Bit Value	Description
				the clock).
			3:2	Not used.
	AGC		1	Enables the automatic gain control if set to '1'. The sync amplitude is measured and compared with a reference and a PWM output signal (Gain_control) is used to control an external voltage controlled amplifier (see chapter 5). If set to a '0' the external voltage controlled amplifier gain is set manually using register $04 (PGA_control).
	ABL		0	Enables the automatic black level if set to '1'. The back porch value is measured and subtracted from the composite video (effectively removing the sync pulses from the luma output). If ABL is turned off, a fixed DC offset set by registers $30 and $31 is subtracted from the output.
Procamp				
$08-$0F				**Proc-amp registers $08-$0F apply if the video standard is NTSC-M (either manually or automatically set).**
$08	**Sub_Luma_value_NTSC_1**	R/W	7:0	Value subtracted from luma output (to remove synchronizing pulses), if ABL = 0 (Control3[0]). 10 bit word = ({Sub_Luma_value_NTSC_2[1:0],Sub_Luma_value_NTSC_1[7:0]}). Default value = 150_{10}.
$09	**Sub_Luma_value_NTSC_2**	R/W	1:0	
$0A	**Ygain_value_NTSC_1**	R/W	7:0	Luma gain control. 10 bit word = ({Ygain_value_NTSC_2[1:0],Ygain_value_NTSC_1[7:0]}). Default value = 746_{10}.
$0B	**Ygain_value_NTSC_2**	R/W	1:0	
$0C	**Ugain_value_NTSC_1**	R/W	7:0	Chroma (B-Y) gain control. 10 bit word = ({Ugain_value_NTSC_2[1:0],Ugain_value_NTSC_1[7:0]}). Default value = 512_{10}.
$0D	**Ugain_value_NTSC_2**	R/W	1:0	
$0E	**Vgain_value_NTSC_1**	R/W	7:0	Chroma (R-Y) gain control. 10 bit word = ({Ugain_value_NTSC_2[1:0],Ugain_value_NTSC_1[7:0]}). Default value = 512_{10}.
$0F	**Vgain_value_NTSC_2**	R/W	1:0	
$10-$18				**Proc-amp registers $10-$18 apply if the video standard is PAL (either manually or automatically set).**
$10	**Sub_Luma_value_PAL_1**	R/W	7:0	Value subtracted from luma output (to remove synchronizing pulses), if ABL = 0 (Control3[0]). 10 bit word = ({Sub_Luma_value_PAL_2[1:0],Sub_Luma_value_PAL_1[7:0]}). Default value = 150_{10}.
$11	**Sub_Luma_value_PAL_2**	R/W	1:0	
$12	**Ygain_value_PAL_1**	R/W	7:0	Luma gain control. 10 bit word = ({Ygain_value_PAL_2[1:0],Ygain_value_PAL_1[7:0]}). Default value = 746_{10}.
$13	**Ygain_value_PAL_2**	R/W	1:0	
$14	**Ugain_value_PAL_1**	R/W	7:0	Chroma (B-Y) gain control. 10 bit word = ({Ugain_value_PAL_2[1:0],Ugain_value_PAL_1[7:0]}). Default value = 512_{10}.
$15	**Ugain_value_PAL_2**	R/W	1:0	
$16	**Vgain_value_PAL_1**	R/W	7:0	Chroma (R-Y) gain control. 10 bit word = ({Ugain_value_PAL_2[1:0],Ugain_value_PAL_1[7:0]}). Default value = 512_{10}.
$17	**Vgain_value_PAL_2**	R/W	1:0	
$18-$1F				**Proc-amp registers $18-$1F apply if the video standard is HD (either manually or automatically set).**
$18	**Sub_Luma_value_HD_1**	R/W	7:0	Value subtracted from luma output (to remove synchronizing pulses), if ABL = 0 (Control3[0]). 10 bit word = ({Sub_Luma_value_HD_2[1:0],Sub_Luma_value_HD_1[7:0]}). Default value = 150_{10}.
$19	**Sub_Luma_value_HD_2**	R/W	1:0	
$1A	**Ygain_value_HD_1**	R/W	7:0	Luma gain control. 10 bit word = ({Ygain_value_HD_2[1:0],Ygain_value_HD_1[7:0]}). Default value = 746_{10}.
$1B	**Ygain_value_HD_2**	R/W	1:0	
$1C	**Ugain_value_HD_1**	R/W	7:0	Chroma (B-Y) gain control. 10 bit word = ({Ugain_value_HD_2[1:0],Ugain_value_HD_1[7:0]}). Default value = 512_{10}.
$1D	**Ugain_value_HD_2**	R/W	1:0	
$1E	**Vgain_value_HD_1**	R/W	7:0	Chroma (R-Y) gain control. 10 bit word = ({Ugain_value_HD_2[1:0],Ugain_value_HD_1[7:0]}). Default value = 512_{10}.
$1F	**Vgain_value_HD_2**	R/W	1:0	
SPG				

Register Offset	Register Name	R/W	Bit Value	Description
$20	**Hcount_length_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hcount Length is preset according to the selected standard. If set to '0', Hcount Length can be programmed manually using these 2 registers: ({Hcount Length_2[3:0], Hcount Length_1[7:0]}). The value is the total number of pixels per line - 1.
$21	**Hcount_length_2**	R/W	3:0	
$22	**Hout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hout_start is preset according to the selected standard. If set to '0', Hout_start can be programmed manually using these 2 registers: ({Hout_start_2[3:0], Hout_start_1[7:0]}). The value is the position of the falling edge of the Hout sync pulse w.r.t. to the falling edge of the input horizontal sync pulse.
$23	**Hout_start_2**	R/W	3:0	
$24	**Hout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hout_end is preset according to the selected standard. If set to '0', Hout_end can be programmed manually using these 2 registers: ({Hout_end_2[3:0], Hout_end_1[7:0]}). The value is the position of the rising edge of the Hout sync pulse w.r.t. to the falling edge of the input horizontal sync pulse.
$25	**Hout_end_2**	R/W	3:0	
$26	**HBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' HBlank_start is preset according to the selected standard. If set to '0', HBlank_start can be programmed manually using these 2 registers: ({HBlank_start_2[3:0], HBlank_start_1[7:0]}). The value is the position of the beginning of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$27	**HBlank_start_2**	R/W	3:0	
$28	**HBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' HBlank_end is preset according to the selected standard. If set to '0', HBlank_end can be programmed manually using these 2 registers: ({HBlank_end_2[3:0], HBlank_end_1[7:0]}). The value is the position of the end of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$29	**HBlank_end_2**	R/W	3:0	
$2A	**Halfline_set_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Halfline_set is preset according to the selected standard. If set to '0', Halfline_set can be programmed manually using these 2 registers: ({Halfline_set_2[3:0], Halfline_set_1[7:0]}). The value is the position of the beginning of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$2B	**Halfline_set_2**	R/W	3:0	
$2C	**Burst_gate_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate start is preset according to the selected standard. If set to '0', Burst gate start can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse for the beginning of the burst gate.
$2D	**Burst_gate_start_2**	R/W	3:0	
$2E	**Burst_gate_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate end is preset according to the selected standard. If set to '0', Burst gate end can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse until the end of the burst gate.
$2F	**Burst_gate_end_2**	R/W	3:0	
$30	**Vout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout_start is preset according to the selected standard. If set to '0', Vout start can be programmed manually using these 2 registers: ({Vout_start_2[2:0], Vout_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Vout output.
$31	**Vout_start_2**	R/W	2:0	
$32	**Vout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout_end is preset according to the selected standard. If set to '0', Vout end can be programmed manually using these 2 registers: ({Vout_end_2[2:0], Vout_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Vout output.
$33	**Vout_end_2**	R/W	2:0	
$34	**Vout2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout2_start is preset according to the selected standard. If set to '0', Vout2 start can be programmed manually using these 2 registers: ({Vout2_start_2[2:0], Vout2_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Vout output for the interlaced field. For non-interlaced formats this register should be set to the same value as Vout_start.
$35	**Vout2_start_2**	R/W	2:0	
$36	**Vout2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout2_end is preset according to the selected standard. If set to '0', Vout2 end can be
$37	**Vout2_end_2**	R/W	2:0	

Register Offset	Register Name	R/W	Bit Value	Description
				programmed manually using these 2 registers: ({Vout2_end_2[2:0], Vout2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Vout output for the interlaced field. For non-interlaced formats this register should be set to the same value as Vout_end.
$38	**Fout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Fout_start is preset according to the selected standard. If set to '0', Fout start can be programmed manually using these 2 registers: ({Fout_start_2[2:0], Fout_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Fout output. This register is only valid for interlaced video formats.
$39	**Fout_start_2**	R/W	2:0	
$3A	**Fout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Fout_end is preset according to the selected standard. If set to '0', Fout end can be programmed manually using these 2 registers: ({Fout_end_2[2:0], Fout_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Fout output. This register is only valid for interlaced video formats.
$3B	**Fout_end_2**	R/W	2:0	
$3C	**VBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank_start is preset according to the selected standard. If set to '0', VBlank start can be programmed manually using these 2 registers: ({VBlank_start_2[2:0], VBlank_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of vertical blanking.
$3D	**VBlank_start_2**	R/W	2:0	
$3E	**VBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank_end is preset according to the selected standard. If set to '0', VBlank_end can be programmed manually using these 2 registers: ({VBlank_end_2[3:0], VBlank_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of vertical blanking.
$3F	**VBlank_end_2**	R/W	2:0	
$40	**VBlank2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank2_start is preset according to the selected standard. If set to '0', VBlank2 start can be programmed manually using these 2 registers: ({VBlank2_start_2[2:0], VBlank2_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$41	**VBlank2_start_2**	R/W	2:0	
$42	**VBlank2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank2_end is preset according to the selected standard. If set to '0', VBlank2 end can be programmed manually using these 2 registers: ({VBlank2_end_2[2:0], VBlank2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$43	**VBlank2_end_2**	R/W	2:0	
$44	**SVBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank_start is preset according to the selected standard. If set to '0', SVBlank start can be programmed manually using these 2 registers: ({SVBlank_start_2[2:0], SVBlank_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of short vertical blanking.
$45	**SVBlank_start_2**	R/W	2:0	
$46	**SVBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank_end is preset according to the selected standard. If set to '0', SVBlank_end can be programmed manually using these 2 registers: ({SVBlank_end_2[3:0], SVBlank_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of short vertical blanking.
$47	**SVBlank_end_2**	R/W	2:0	
$48	**SVBlank2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank2_start is preset according to the selected standard. If set to '0', SVBlank2 start can be programmed manually using these 2 registers: ({SVBlank2_start_2[2:0], SVBlank2_start_1[7:0]}).
$49	**SVBlank2_start_2**	R/W	2:0	

Register Offset	Register Name	R/W	Bit Value	Description
				The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of short vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$4A	**SVBlank2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank2_end is preset according to the selected standard. If set to '0', SVBlank2 end can be programmed manually using these 2 registers: ({SVBlank2_end_2[2:0], SVBlank2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of short vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$4B	**SVBlank2_end_2**	R/W	2:0	
$4C	**FSc_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the subcarrier frequency seed is preset according to the selected standard. If set to '0', the subcarrier frequency seed can be programmed manually using these 4 registers: ({FSc_1[7:0], FSc_2[7:0], FSc_3[7:0], FSc_4[7:0]}). The seed is a 32 bit number and FSc_1[7] is the MSB. Default value is 55693156_H
$4D	**FSc_2**	R/W	7:0	
$4E	**FSc_3**	R/W	7:0	
$4F	**FSc_4**	R/W	7:0	
AGC_control				
$63	**AGC_Default_MSB**	R/W	1:0	Value used for the PWM AGC gain control when AGC is turned off (Control Register 3 bit 1 = '0'). Effectively is the 0dB gain value for the programmable gain amplifier.({AGC_Default_MSB[1:0],AGC_Default_1[7:0]}). Default value = 368_{10}.
$60	**AGC_Default_1**	R/W	7:0	
$63	**AGC_Default_MSB**	R/W	4:3	Starting value used for the PWM AGC gain control when AGC is turned on (Control Register 3 bit 1 = '1') and the video standard is SD or 960H. ({AGC_Default_MSB[4:3]AGC_SD_PU_1[7:0]}). Default value = 388_{10}.
$61	**AGC_SD_PU_1**	R/W	7:0	
$63	**AGC_Default_MSB**	R/W	7:6	Starting value used for the PWM AGC gain control when AGC is turned on (Control Register 3 bit 1 = '1') and the video standard is HD. ({AGC_Default_MSB[7:6]AGC_SD_PU_1[7:0]}). Default value = 500_{10}.
$62	**AGC_HD_PU_1**	R/W	7:0	
$66	**AGC_Limit_MSB**	R/W	1:0	Lower limit for the AGC PWM value when AGC is turned on (Control Register 3 bit 1 = '1'). ({AGC_Limit_MSB[1:0]AGC_LL_1[7:0]}). Default value = 348_{10}.
$64	**AGC_LL_1**	R/W	7:0	
$66	**AGC_Limit_MSB**	R/W	4:3	Upper limit for the AGC PWM value when AGC is turned on (Control Register 3 bit 1 = '1'). ({AGC_Limit_MSB[4:3]AGC_UL_1[7:0]}). Default value = 552_{10}.
$65	**AGC_UL_1**	R/W	7:0	
Status				
$6D	**Status**	R	7:2	Not used
			1	Burst lock detect.
			0	Horizontal lock detect.
$6E	**Video standard**	R	7:5	Reports the detected format.
				Bits 7:5 — Video format
				000 — NTSC/PAL
				011 — aCVi2
				100 — AHD
				101 — HD-CVI
				110 — HD-TVI
				111 — Invalid format
			4:0	Reports the detected standard.
				Bits 4:0 — Video standard
				00000 — 720p/25
				00001 — 720p/30
				00010 — 720p/50
				00100 — 720p/60
				00110 — 1080p/25
				01000 — 1080p/30
				10000 — NTSC-M
				10100 — PAL
				11111 — Invalid standard

Table 5 Register description.

10. Default register settings

Parameter	720p/25	720p/30	720p/50	720p/59	720p/60
Hcount_length	12'd3959	12'd3299	12'd1979	12'd1649	12'd1649
Hout_start	12'd98	12'd98	12'd98	12'd98	12'd98
Hout_end	12'd178	12'd178	12'd178	12'd178	12'd178
BP_gate_start	12'd185	12'd185	12'd185	12'd185	12'd185
BP_gate_end	12'd217	12'd217	12'd217	12'd217	12'd217
HBlank_start	12'd2196	12'd2196	12'd2196	12'd2196	12'd2196
HBlank_end	12'd276	12'd276	12'd276	12'd276	12'd276
Halfline_set	12'd1980	12'd1980	12'd1980	12'd1980	12'd1980
White_gate_start	12'd297	12'd297	12'd297	12'd297	12'd297
White_gate_end	12'd329	12'd329	12'd329	12'd329	12'd329
Vout_start	11'd747	11'd747	11'd747	11'd747	11'd747
Vout_end	11'd2	11'd2	11'd2	11'd2	11'd2
Vout2_start	11'd747	11'd747	11'd747	11'd747	11'd747
Vout2_end	11'd2	11'd2	11'd2	11'd2	11'd2
Fout_start	11'd0	11'd0	11'd0	11'd0	11'd0
Fout_end	11'd0	11'd0	11'd0	11'd0	11'd0
VBlank_start	11'd742	11'd742	11'd742	11'd742	11'd742
VBlank_end	11'd22	11'd22	11'd22	11'd22	11'd22
VBlank2_start	11'd742	11'd742	11'd742	11'd742	11'd742
VBlank2_end	11'd22	11'd22	11'd22	11'd22	11'd22
SVBlank_start	11'd742	11'd742	11'd742	11'd742	11'd742
SVBlank_end	11'd4	11'd4	11'd4	11'd4	11'd4
SVBlank2_start	11'd742	11'd742	11'd742	11'd742	11'd742
SVBlank2_end	11'd4	11'd4	11'd4	11'd4	11'd4

Table 6 Default register settings: aCVi, 720p formats.

Parameter	1080p/24	1080p/25	1080p/29	1080p/30	1080i/50	1080i/59	1080i/60
Hcount_length	12'd2749	12'd2639	12'd2199	12'd2199	12'd2639	12'd2199	12'd2199
Hout_start	12'd110	12'd110	12'd110	12'd110	12'd110	12'd110	12'd110
Hout_end	12'd190	12'd190	12'd190	12'd190	12'd190	12'd190	12'd190
BP_gate_start	12'd160	12'd160	12'd160	12'd160	12'd160	12'd160	12'd160
BP_gate_end	12'd192	12'd192	12'd192	12'd192	12'd192	12'd192	12'd192
HBlank_start	12'd2196	12'd2196	12'd2196	12'd2196	12'd2196	12'd2196	12'd2196
HBlank_end	12'd276	12'd276	12'd276	12'd276	12'd276	12'd276	12'd276
Halfline_set	12'd1275	12'd1275	12'd1275	12'd1275	12'd1275	12'd1275	12'd1275
White_gate_start	12'd297	12'd297	12'd297	12'd297	12'd297	12'd297	12'd297
White_gate_end	12'd329	12'd329	12'd329	12'd329	12'd329	12'd329	12'd329
Vout_start	11'd1123	11'd1123	11'd1123	11'd1123	11'd1123	11'd1123	11'd1123
Vout_end	11'd3	11'd3	11'd3	11'd3	11'd2	11'd2	11'd2
Vout2_start	11'd1123	11'd1123	11'd1123	11'd1123	11'd560	11'd560	11'd560
Vout2_end	11'd3	11'd3	11'd3	11'd3	11'd564	11'd564	11'd564
Fout_start	11'd0	11'd0	11'd0	11'd0	11'd1123	11'd1123	11'd1123
Fout_end	11'd0	11'd0	11'd0	11'd0	11'd560	11'd560	11'd560
VBlank_start	11'd1119	11'd1119	11'd1119	11'd1119	11'd1121	11'd1121	11'd1121
VBlank_end	11'd39	11'd39	11'd39	11'd39	11'd20	11'd20	11'd20
VBlank2_start	11'd1119	11'd1119	11'd1119	11'd1119	11'd558	11'd558	11'd558
VBlank2_end	11'd39	11'd39	11'd39	11'd39	11'd583	11'd583	11'd583
SVBlank_start	11'd1118	11'd1118	11'd1118	11'd1118	11'd1123	11'd1123	11'd1123
SVBlank_end	11'd4	11'd4	11'd4	11'd4	11'd4	11'd4	11'd4
SVBlank2_start	11'd1118	11'd1118	11'd1118	11'd1118	11'd560	11'd560	11'd560
SVBlank2_end	11'd4	11'd4	11'd4	11'd4	11'd566	11'd566	11'd566

Table 7 Default register settings: aCVi, 1080p/i formats.

Parameter	NTSC	PAL	NTSC-960H	PAL-960H
Hcount_length	12'd857	12'd863	12'd1143	12'd1151
Hout_start	12'd41	12'd46	12'd41	12'd61
Hout_end	12'd105	12'd110	12'd126	12'd146
BP_gate_start	12'd101	12'd101	12'd135	12'd135
BP_gate_end	12'd117	12'd117	12'd151	12'd151
HBlank_start	12'd21	12'd24	12'd21	12'd25
HBlank_end	12'd169	12'd168	12'd169	12'd190
Halfline_set	12'd429	12'd432	12'd572	12'd576
White_gate_start	12'd0	12'd0	12'd0	12'd0
White_gate_end	12'd0	12'd0	12'd0	12'd0
Vout_start	11'd523	11'd623	11'd523	11'd623
Vout_end	11'd1	11'd1	11'd1	11'd1
Vout2_start	11'd261	11'd310	11'd261	11'd310
Vout2_end	11'd264	11'd313	11'd264	11'd313
Fout_start	11'd523	11'd623	11'd523	11'd623
Fout_end	11'd261	11'd310	11'd261	11'd310
VBlank_start	11'd520	11'd621	11'd520	11'd621
VBlank_end	11'd15	11'd20	11'd15	11'd20
VBlank2_start	11'd257	11'd311	11'd257	11'd311
VBlank2_end	11'd278	11'd333	11'd278	11'd333
SVBlank_start	11'd519	11'd619	11'd519	11'd619
SVBlank_end	11'd3	11'd3	11'd3	11'd3
SVBlank2_start	11'd256	11'd307	11'd256	11'd307
SVBlank2_end	11'd266	11'd316	11'd266	11'd316

Table 8 Default register settings: SD formats.