PT52

Advanced Composite Video Interface: Decoder IP Core

User Manual

Revision 0.1
22nd March 2020

Revisions

Date	Revisions	Version
22-03-2020	First Draft.	0.1

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1. Introduction

PT52 is an aCVi®[1] decoder IP (intellectual property) core compatible with the aCVi® Advanced Composite Video Interface (revision 2).

aCVi is a method to transmit high definition video over long distances (>300m) of low cost coaxial or twisted-pair cable. SingMai are proposing aCVi as an open standard. The current version of the standard may be found here:
https://www.singmai.com/Documents/aCVi%20Format%20Specification.pdf

The encoder IP accepts digital composite aCVi® encoded video which it decodes to a YCbCr 4:2:2 output. PT52 currently supports 720p-25/30/50/59.94/60Hz and 1080p-24/25/29.97/30Hz HD video formats.

Control and status registers are written to and read from using a conventional 8 bit wide microprocessor interface.

The intellectual property block is provided as RTL compliant Verilog-2001 source code for FPGAs from all vendors or for ASICs.

Typical resource usage for an Altera FPGA is shown in Table 1.

Logic Cells	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers

Table 1 PT52 Altera FPGA resource requirements

An approximate equivalent for ASIC resource usage is TBA LCs (logic cell only compile for Altera FPGA) x 14 ~ TBA 2 input NAND gate equivalent. The memory is TBAkb of single port ROM (512 x 24).

1 aCVi® is a registered trademark of SingMai Electronics Ltd.

2. PT52 Module description

The PT52 aCVi® decoder IP core comprises 10 Verilog modules in a hierarchical structure, (see Table 2).

PT52_decoder.v	Register_control.v	
	Demod.v	SinCos.v
	DemodLPF.v	
	SPG.v	Sync_DemodLPF.v
	Line_delays.v	ram_infer_generic.v
	Procamp.v	

Table 2 PT52 Verilog file structure.

The top level file is PT56_encoder.v which, in turn, calls six of the other modules. Three of these modules call a third level of modules.

3. Signal Interconnections

The PT52 signal interconnect diagram is shown in Figure 1.

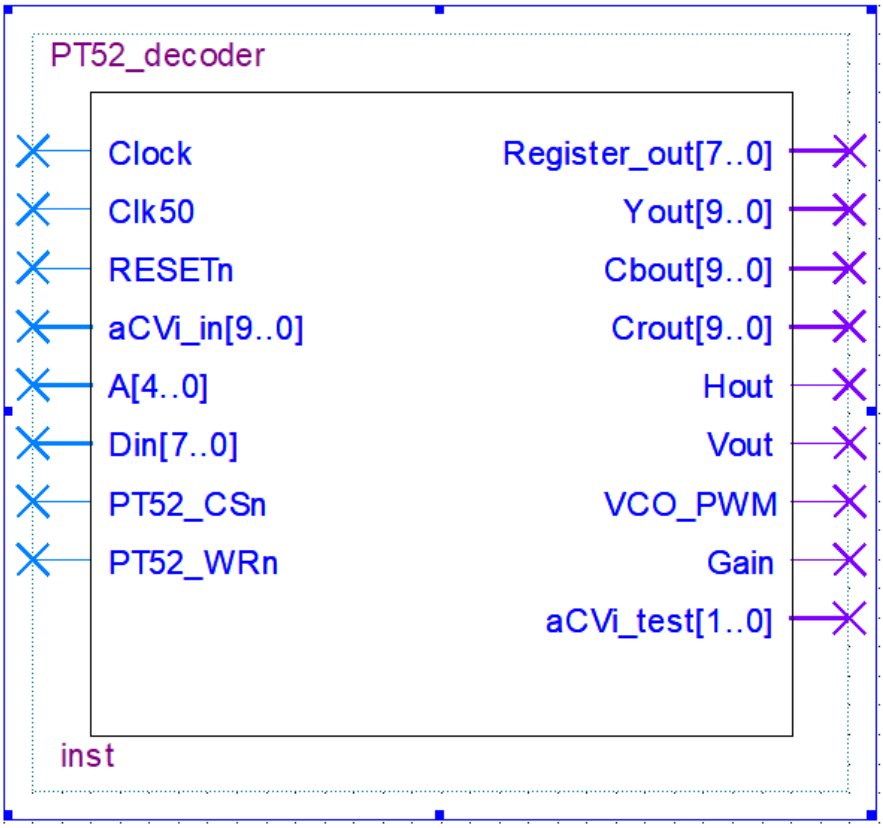

Figure 1 PT52 Block schematic.

The signal descriptions are shown in Table 3, below.

Inputs	
Signal	**Description**
Clock	74.25MHz/74.18MHz clock input from the voltage-controlled oscillator.
Clk50	50MHz clock input used for the video standard measurement.
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all registers.
aCVi[9:0]	Digital composite aCVi input from the ADC, sampled at 'Clock' input frequency. This input is signed 2's complement format.
A[4:0]	Control address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT52_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
PT52_WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers.

Outputs	
Signal	**Description**
Register_out[7:0]	Control output data bus. Outputs the control/status register data selected by the A[4:0] bus.
CSync	Digital composite sync output.
Y_out[9:0]	Decoded luma output. Y_out[9:0] is straight binary; Y[9] is the MSB. The output is valid on the rising edge of 'Clock'.
Cb_out[9:0]	Decoded chroma output. Cb_out[9:0] is offset binary; Cb[9] is the MSB. The output is valid on the rising edge of 'Clock'.
Cr_out[9:0]	Decoded chroma output. Cr_out[9:0] is offset binary; Cr[9] is the MSB. The output is valid on the rising edge of 'Clock'.
H_out	Horizontal sync output. Active low output.
V_out	Vertical sync output. Active low output.
VCO_PWM	Pulse width modulated output used to control the frequency of the voltage-controlled oscillator.
Gain	Pulse width modulated output used to control the analogue voltage controlled amplifier (automatic gain control).

Table 3 PT52 Input/Output signals

The Verilog instantiation of PT52 is shown below:

```
PT52_decoder PT52_decoder_inst
(
.Clock(Clock_sig) ,                     // input  Clock_sig
.Clk50(Clk50_sig) ,                     // input  Clk50_sig
.RESETn(RESETn_sig) ,                   // input  RESETn_sig
.aCVi_in(aCVi_in_sig) ,                 // input [9:0] aCVi_in_sig
.A(A_sig) ,                             // input [4:0] A_sig
.Din(Din_sig) ,                         // input [7:0] Din_sig
.PT52_CSn(PT52_CSn_sig) ,               // input  PT52_CSn_sig
.PT52_WRn(PT52_WRn_sig) ,               // input  PT52_WRn_sig

.Register_out(Register_out_sig) ,       // output [7:0] Register_out_sig
.Yout(Yout_sig) ,                       // output [9:0] Yout_sig
.Cbout(Cbout_sig) ,                     // output [9:0] Cbout_sig
.Crout(Crout_sig) ,                     // output [9:0] Crout_sig
.Hout(Hout_sig) ,                       // output  Hout_sig
.Vout(Vout_sig) ,                       // output  Vout_sig
.VCO_PWM(VCO_PWM_sig) ,                 // output  VCO_PWM_sig
.Gain(Gain_sig) ,                       // output  Gain_sig
.aCVi_test(aCVi_test_sig)               // output [1:0] aCVi_test_sig
);
```

4. aCVi® Overview

The following is a brief overview of the aCVi® revision 2 interface (abbreviated to aCVi® in this document).

aCVi® is a proprietary format, developed by SingMai Electronics, to transmit high definition video over long distances of coaxial or twisted pair cable. aCVi® is an update to the previous version, specifically designed to interface directly to image sensors, although it may also be used to transmit conventional video sources.

A single chip image sensor, as found in almost all non-broadcast cameras, uses a colour filter to 'assign' each sensor pixel one of red, green or blue sensitivities. Because green is where the human eye is most sensitive, there are twice as many green pixels as red and blue (see Figure 2). This means that if your sensor has a horizontal array of 1920 pixels, only 960 of them are green, red or blue pixels, and for the red and blue pixels, each horizontal line is either red or blue. The actual resolution of the sensor to each colour is for green, 960 x 1080 pixels, and for red and blue, 960 x 540 pixels. (A broadcast camera will use three optically aligned sensors, each offering 1920 x 1080 pixels for the three colours). If we refer to the full resolution (e.g. a broadcast camera) as 4:4:4 sampled, a single image sensor actually produces a 2:2:0 output.

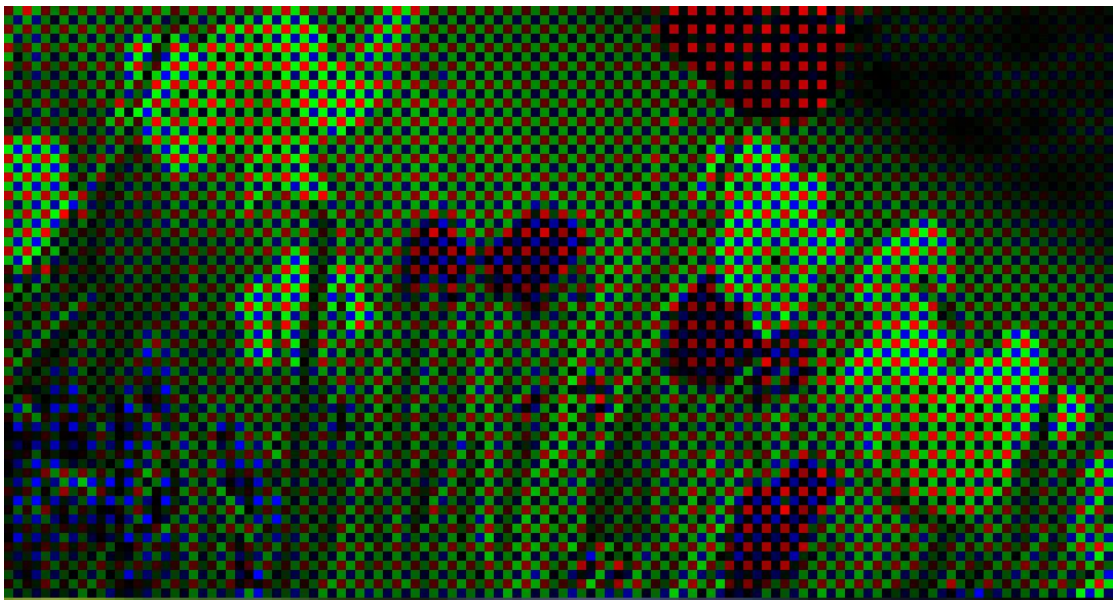

Figure 2 Bayer colour filter.

To conform with video standards (e.g. 1920 x 1080) the additional pixels are interpolated (a technique known as Bayer de-mosaicing) and this function is usually performed in the camera ISP (Image Signal Processor). However this process can produce artifacts into the image (for example see the colour artifacts on the white fence in Figure 3), and also, because it generates more than double the amount of original pixels, more than doubles the bandwidth of the output signal, which exacerbates the problem if the video is required to transmitted long distances.

aCVi® interfaces directly to the single chip image sensor and transmits the RAW 2:2:0 resolution image directly, thereby reducing by more than half the bandwidth of the transmitted signal and achieving higher resolution, lower noise and greater distances.

Figure 3 Left: Original full resolution image. Right: Image after Bayer demosaicing.

The available aCVi® IP cores are shown in Figure 4. The PT56 provides an aCVi® transmitter for RAW or YCbCr (BT1120 style interface) and outputs digital aCVi for a digital to analogue converter (DAC).

The receiver IP core is the PT52. An analogue front end (AFE) conditions the analogue aCVi video before it is converted to digital aCVi in an analogue to digital converter (ADC). The PT52 decodes the aCVi input (RAW or YCbCr format) into a YCbCr output.

Figure 4 aCVi IP cores.

5. Analogue Front End

A simplified block diagram of the PT52 encoder is shown in Figure 6. U9 and U15 are differential receivers, U9 for twisted pair cable inputs and U15 for coaxial cable inputs (U15 treats the coaxial cable as pseudo-differential to achieve some degree of hum reduction).

The outputs of the differential receivers are single ended, and AC coupled into U10 which is a voltage-controlled amplifier (VCA). The AC coupled outputs are biased at a mid-rail voltage (2.5VDC) which is provided by U13a. The VCA provides the gain for the automatic gain control loop. The required gain is determined by the PT52 which provides a pulse width modulated (PWM) output ('Gain') which is low pass filtered and buffered by U13b to provide the analogue control voltage to the VCA. The gain/control voltage response is shown in Figure 5.

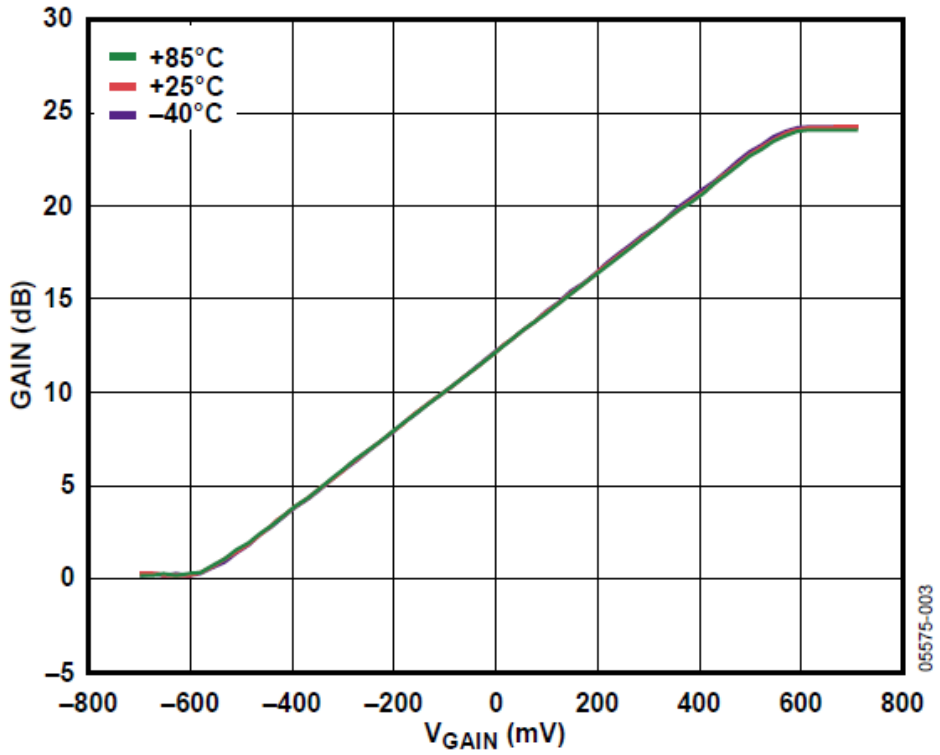

Figure 5 Voltage controlled amplifier gain/control voltage response.

The output of the VCA is AC coupled and biased to the mid-rail point (1.5VDC) of the analogue to digital converter (ADC).

The ADC schematic is shown in Figure 7. The ADC is a dual 10-bit ADC, U19, an AD9216, which is clocked at 74.25MHz. The dual ADC is clocked in anti-phase to ease the ADC requirements. For sample rates of 74.25MHz and below a single ADC (ADC A) is used. For sample rates higher than this each ADC is clocked at half the sample rate but 180° out of phase. The two ADC outputs are then interleaved at the full sample rate (for example, each ADC is clocked at 74.25MHz, but out of phase, giving an effective sample rate of 148.5MHz|. The output from the ADCs is 2's complement coded 10-bit digital aCVi video.

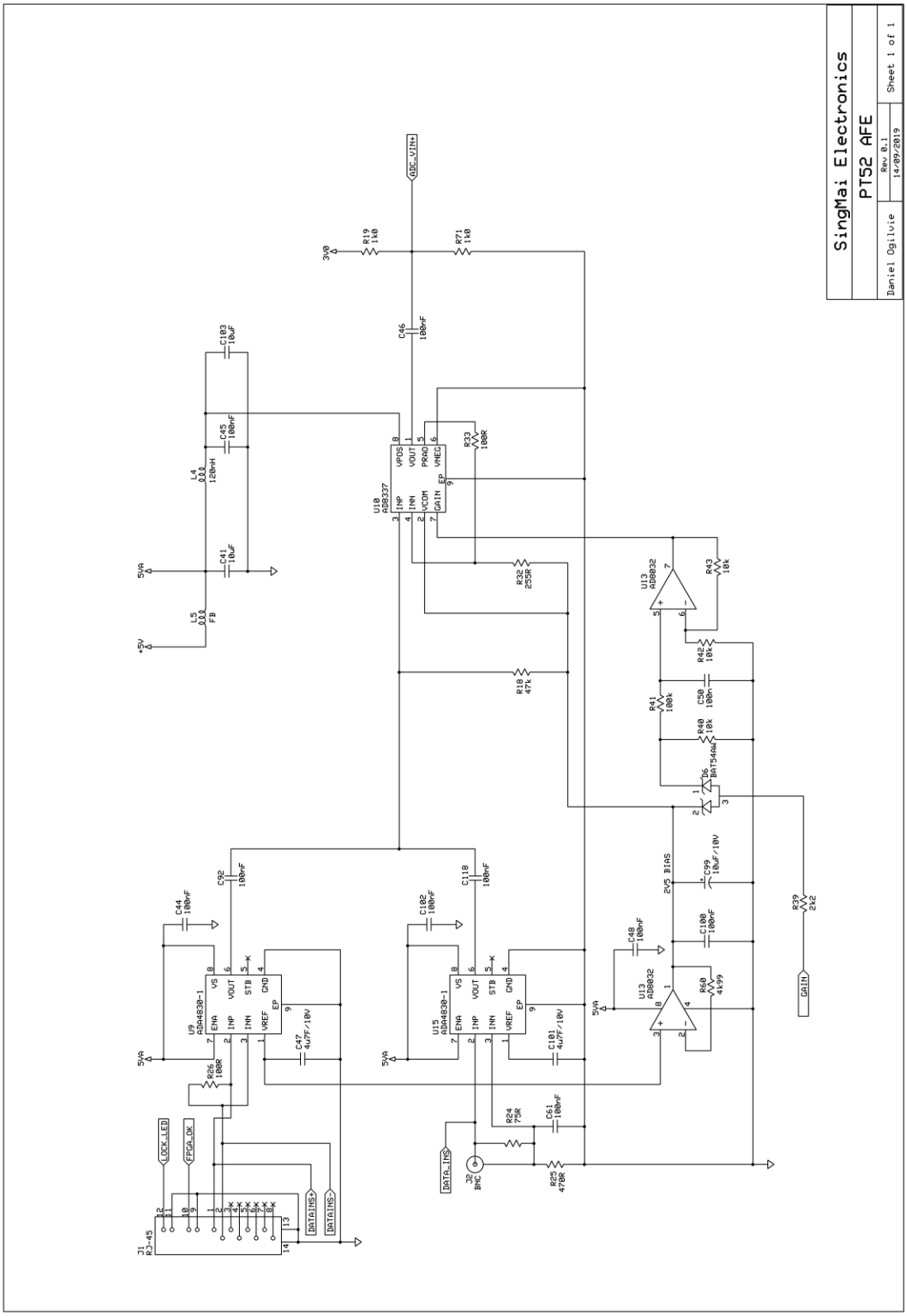

Figure 6 PT52 AFE schematic.

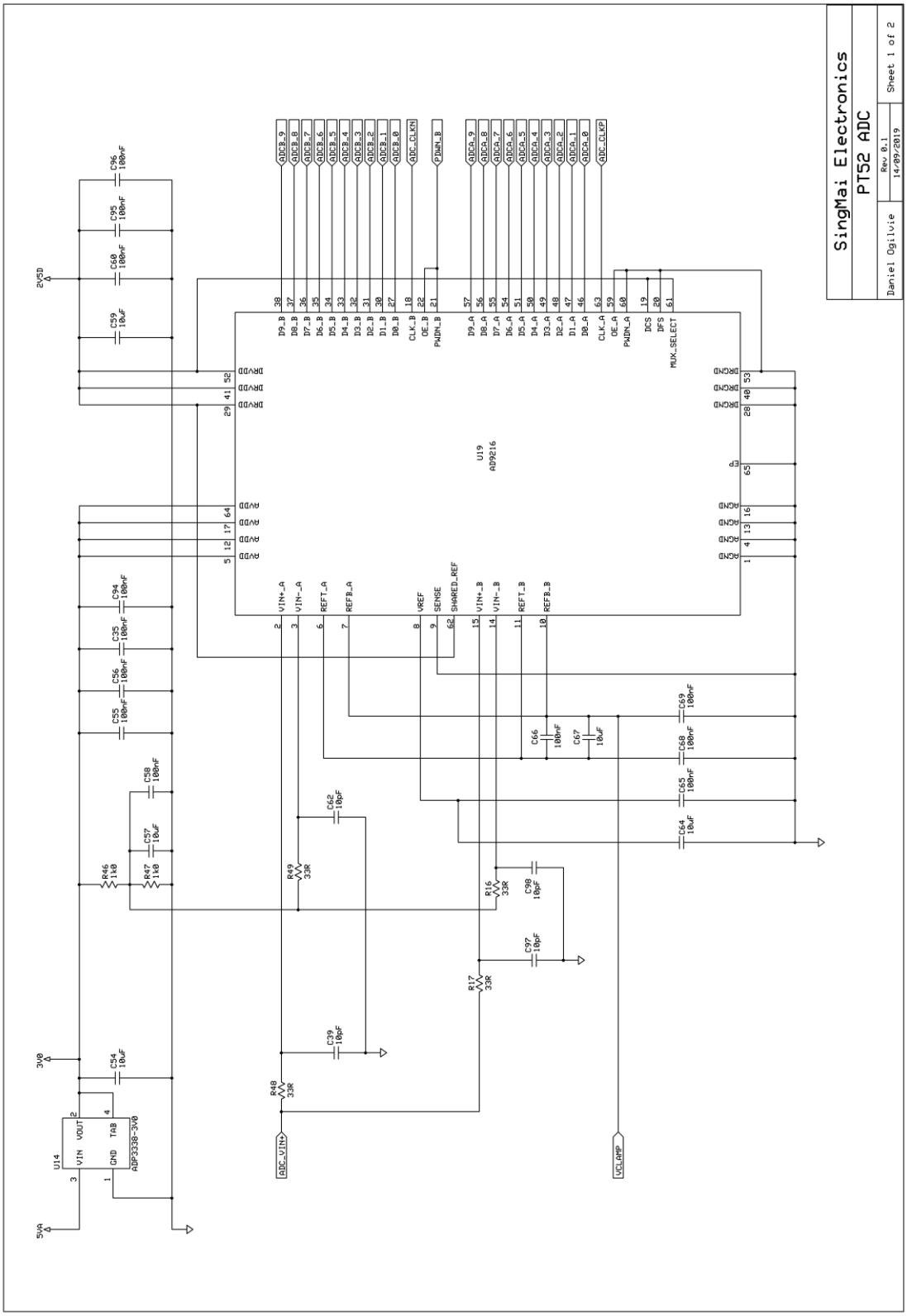

Figure 7 PT52 ADC schematic.

6. Clock generation

The PT52 requires the clock input to phase aligned with the horizontal line frequency. To achieve this the clock is generated by a voltage-controlled oscillator whose frequency is controlled by the PT52 IP core (see Figure 8).

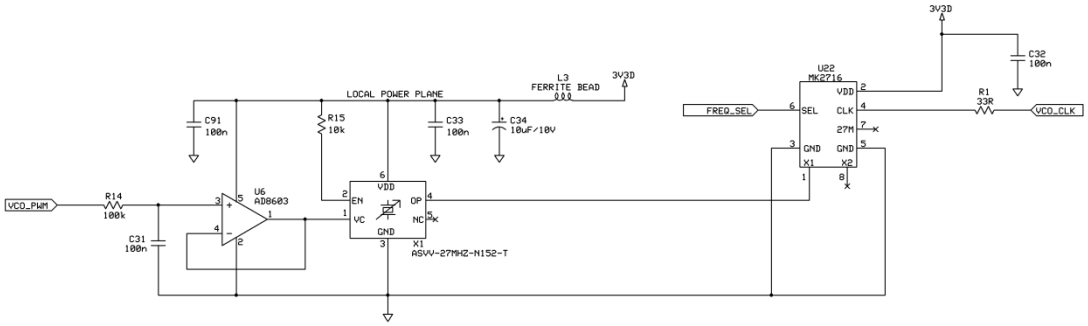

Figure 8 Voltage controlled oscillator.

The PWM signal is low pass filtered (R14 and C31) and buffered (U6), to become the analogue control voltage to a VCXO (voltage-controlled crystal oscillator – X1).

7. Technical Overview

The interconnections between the PT52 IP core and the external peripherals are shown in Figure 9 and the simplified PT52 block diagram is shown in Figure 10. The description of the Verilog modules follows.

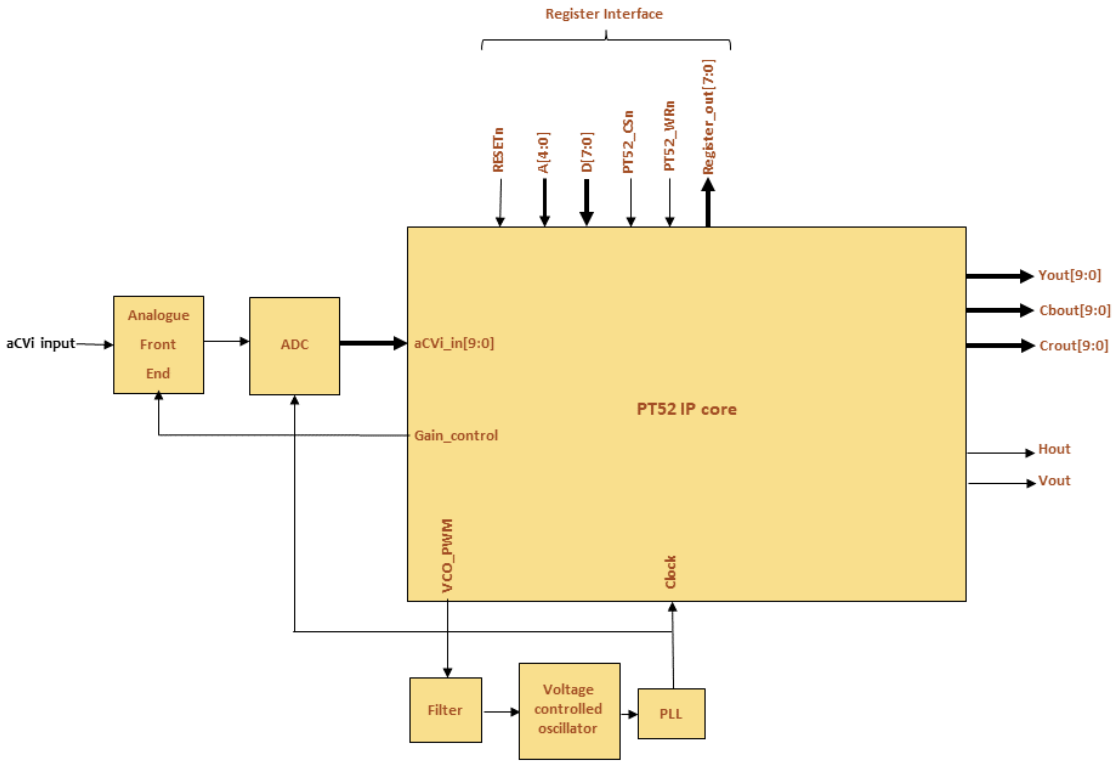

Figure 9 PT52 peripherals.

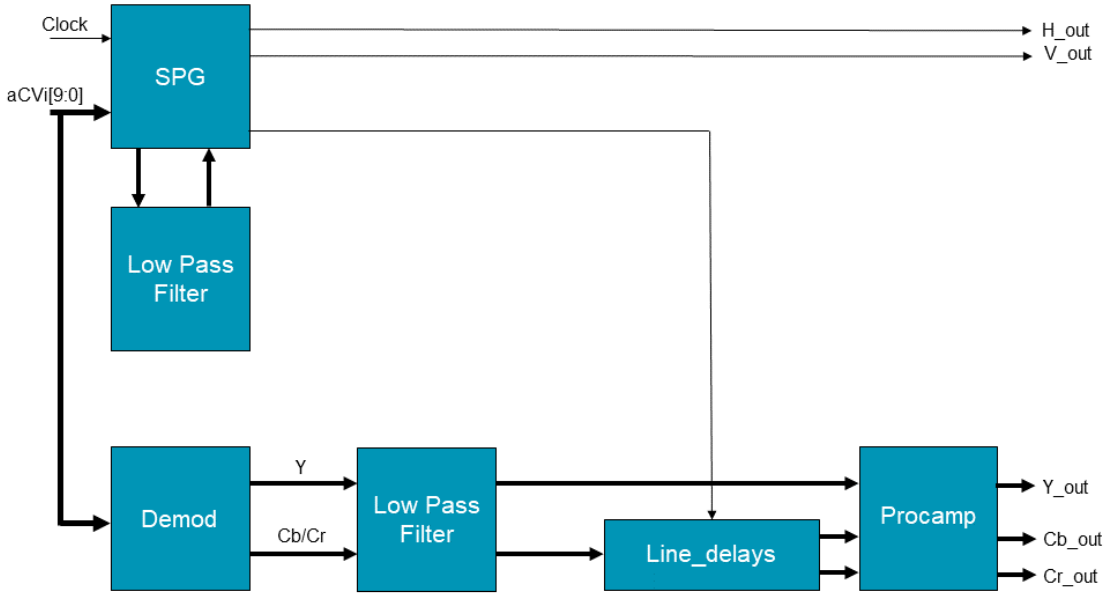

Figure 10 PT52 Block diagram.

PT55_encoder.v

This is the top-level design file and it interconnects all the following modules. Figure 11 shows the spectrum of the aCVi video input. The aCVi input is 10-bit 2'complement video sampled at 74.25MHz/74.18MHz.

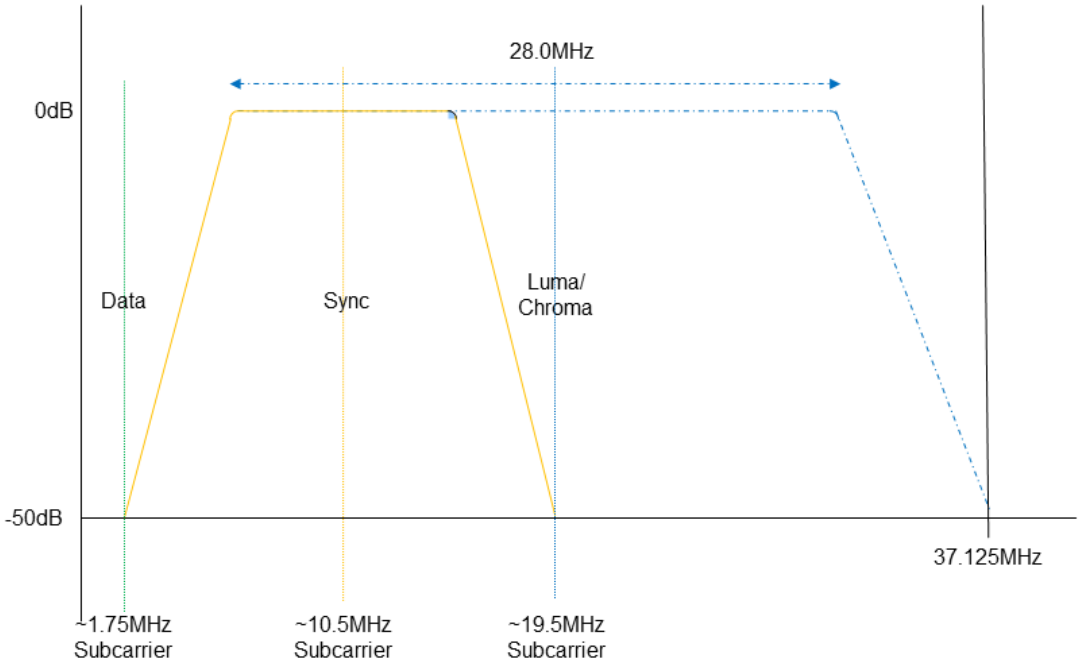

Figure 11 aCVi spectrum.

Register_control.v

A conventional 8-bit microprocessor style control interface is used to write and read to the PT52 control registers. Details of the interface may be found in Chapter 9 and the register descriptions may be found in Chapter 10.

SPG.v

The digital aCVi video is received by the SPG.v (Sync Pulse Generator) module. A ratio counter generates the sync subcarrier frequency as shown in Table 4 (approximately 10.5MHz). The top 11 bits of the ratio counter (phase value) address sine and cosine lookup tables. The sine and cosine waveforms are multiplied by the aCVi video input.

Standard	Pixels/line	Line frequency	Clock frequency	Horizontal sync width (clocks)	Broad pulse start position (clocks)	Broad pulse end position (clocks)	Sync Subcarrier frequency
720p/25Hz	3960	18.750kHz	74.25MHz	80	296	3590	10.561875MHz
720p/30Hz	3300	22.500kHz	74.25MHz	80	296	2930	10.51425MHz
720p/50Hz	1980	37.500kHz	74.25MHz	80	296	1610	10.39875MHz
720p/59Hz	1650	44.955kHz	74.18MHz	80	296	1280	10.488012MHz
720p/60Hz	1650	45.000kHz	74.25MHz	80	296	1280	10.4985MHz
1080p/24Hz	2750	27.000kHz	74.25MHz	80	236	1920	10.5111MHz
1080p/25Hz	2640	28.125kHz	74.25MHz	80	236	1920	10.4990625MHz
1080p/29Hz	2200	33.716kHz	74.18MHz	80	236	1920	10.49587912MHz
1080p/30Hz	2200	33.750kHz	74.25MHz	80	236	1920	10.506375MHz

Table 4 aCVi sync standards.

The output of the multipliers is low pass filtered using a 23-tap FIR filter. The response of this filter is shown in Figure 12.

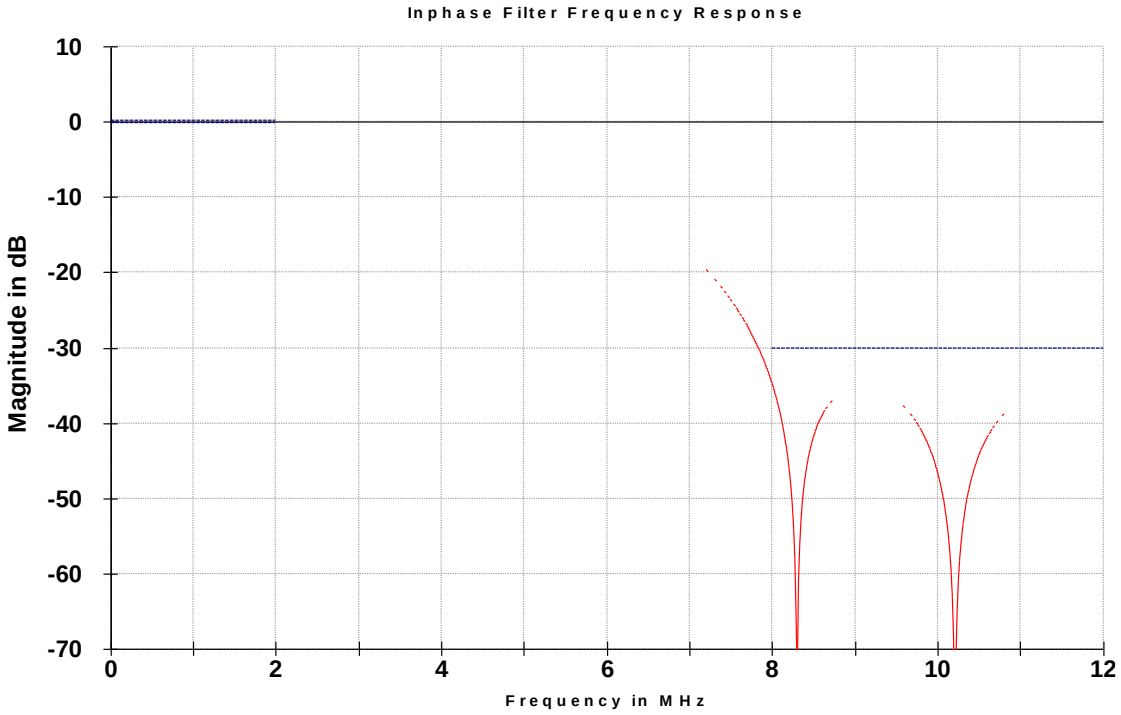

Figure 12 Frequency characteristic of the Sync demodulation low pass filter.

The low pass filtered sine channel is used as the frequency/phase reference to lock the demodulator and the cosine channel is the demodulated sync waveform. The sync pulse generator provides a gating pulse which occurs during the modulated sync burst. 32 samples of the low pass filtered sine waveform are accumulated each horizontal line. When the free-running output of the ratio counter and the frequency and phase of the aCVi input sync are aligned this accumulated value will be zero. Otherwise it adjusts the phase and frequency of the ratio counter until they are.

When the sync demodulator loop is locked, we will have correctly demodulated the sync waveform. The recovered horizontal sync waveform is shown in Figure 13.

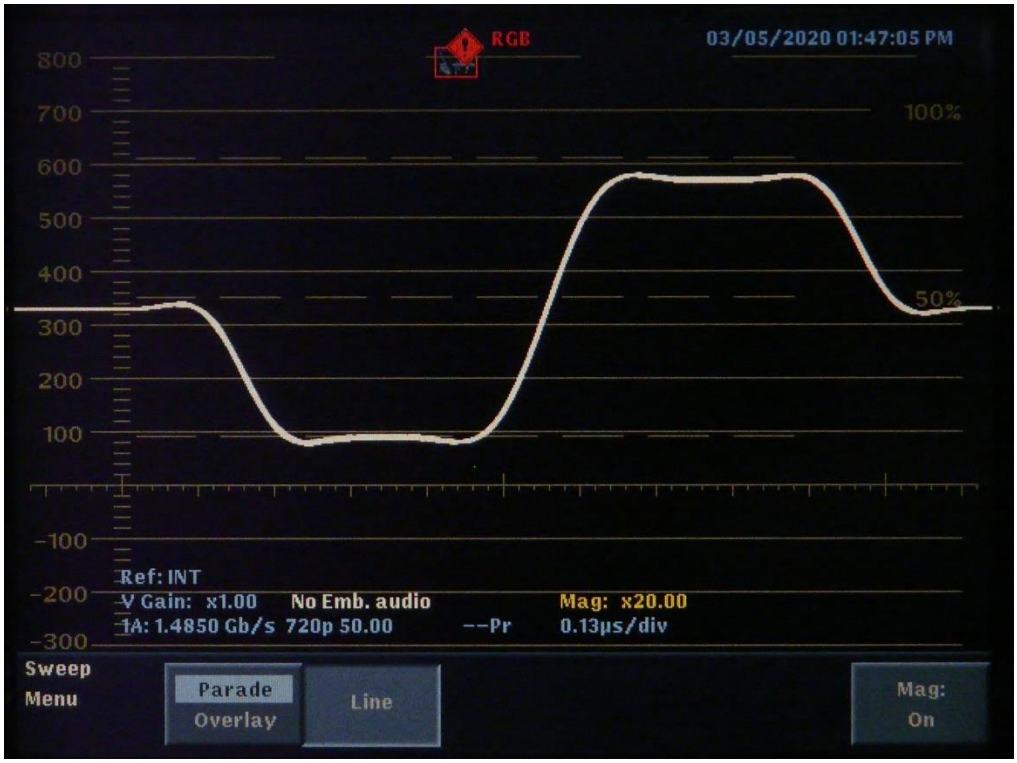

Figure 13 Demodulated horizontal sync waveform.

A free-running counter generates a horizontal sync pulse for the appropriate video standard. 32 of these counts address a lookup table which supplies coefficients to a FIR filter. This filter further reduces noise and its response is shown in Figure 14. The coefficients are multiplied by the low pass filtered cosine channel and accumulated. If the 32 samples align with the sync waveform their accumulated value will be zero. Otherwise the accumulated value is filtered and used to control a pulse width modulated output (VCO_PWM) which in turn adjust the frequency of a voltage-controlled oscillator (see Chapter 6). The frequency of the VCO is therefore adjusted until the free-running and the recovered sync waveforms align.

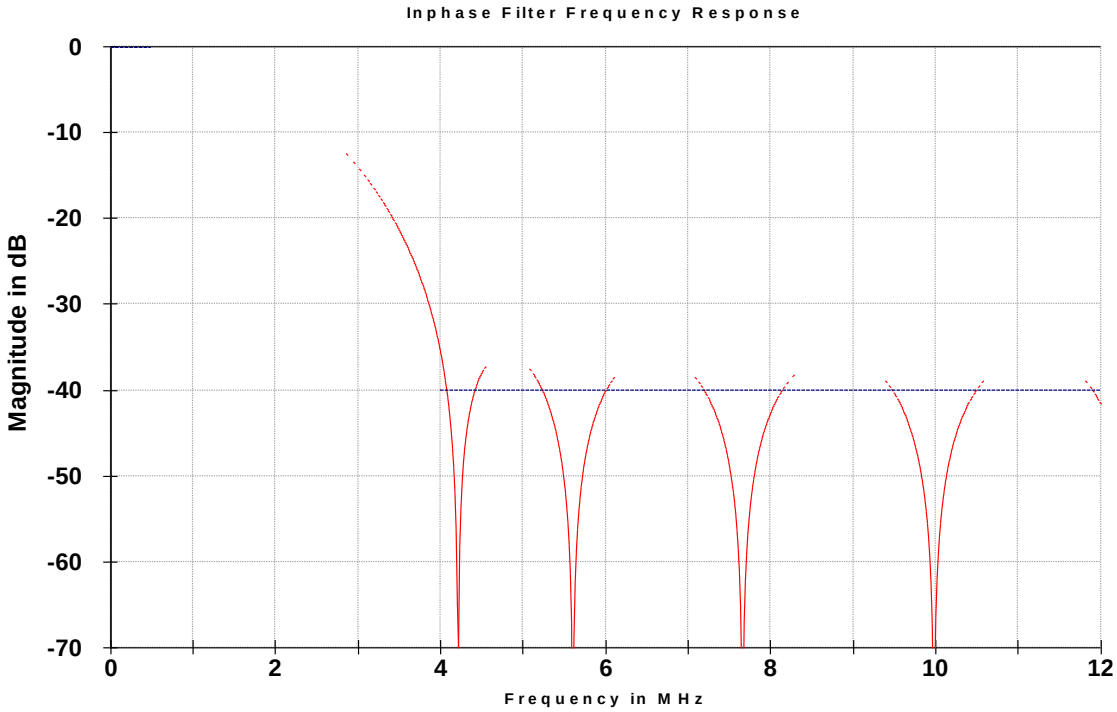

Figure 14 Frequency characteristic of the Sync phase detector.

The vertical sync recovery detects the wide broad pulses (see Figure 15) during the vertical interval by integrating the low pass filtered cosine values and thresholding the integrated values. The narrow horizontal pulses do not pass the threshold, but the wide broad vertical pulses do.

The SPG modules then regenerates the horizontal and vertical timing signals required by the PT52 decoder. The H_out and V_out sync pulses may be moved relative to the video to match and subsequent module's timing requirements.

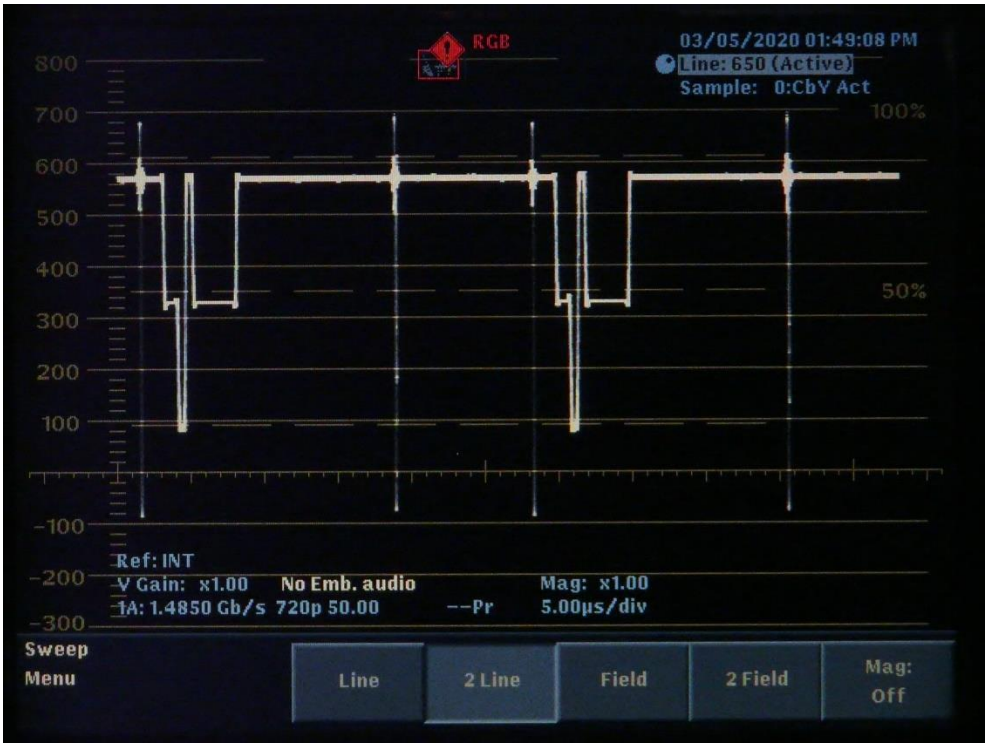

Figure 15 Demodulated Vertical sync waveform.

Demod.v

Another ratio counter generates the video subcarrier value as shown in Table 5.

Standard	Pixels/line	Line frequency	Clock frequency	Burst gate start position (clock periods)			Video Subcarrier frequency
720p/25Hz	3960	18.750kHz	74.25MHz	151			19.509375MHz
720p/30Hz	3300	22.500kHz	74.25MHz	151			19.49625MHz
720p/50Hz	1980	37.500kHz	74.25MHz	151			19.51875MHz
720p/59Hz	1650	44.955kHz	74.18MHz	151			19.488012MHz
720p/60Hz	1650	45.000kHz	74.25MHz	151			19.5075MHz
1080p/24Hz	2750	27.000kHz	74.25MHz	121			19.5075MHz
1080p/25Hz	2640	28.125kHz	74.25MHz	121			19.50487MHz
1080p/29Hz	2200	33.716kHz	74.18MHz	121			19.50487MHz
1080p/30Hz	2200	33.750kHz	74.25MHz	121			19.490625MHz

Table 5 aCVi video parameters.

Sine and Cosine waveforms are generated at this frequency which are then multiplied by the digital aCVi video and low pass filtered. The low pass filter is a 47-tap FIR with a response as shown in Figure 16.

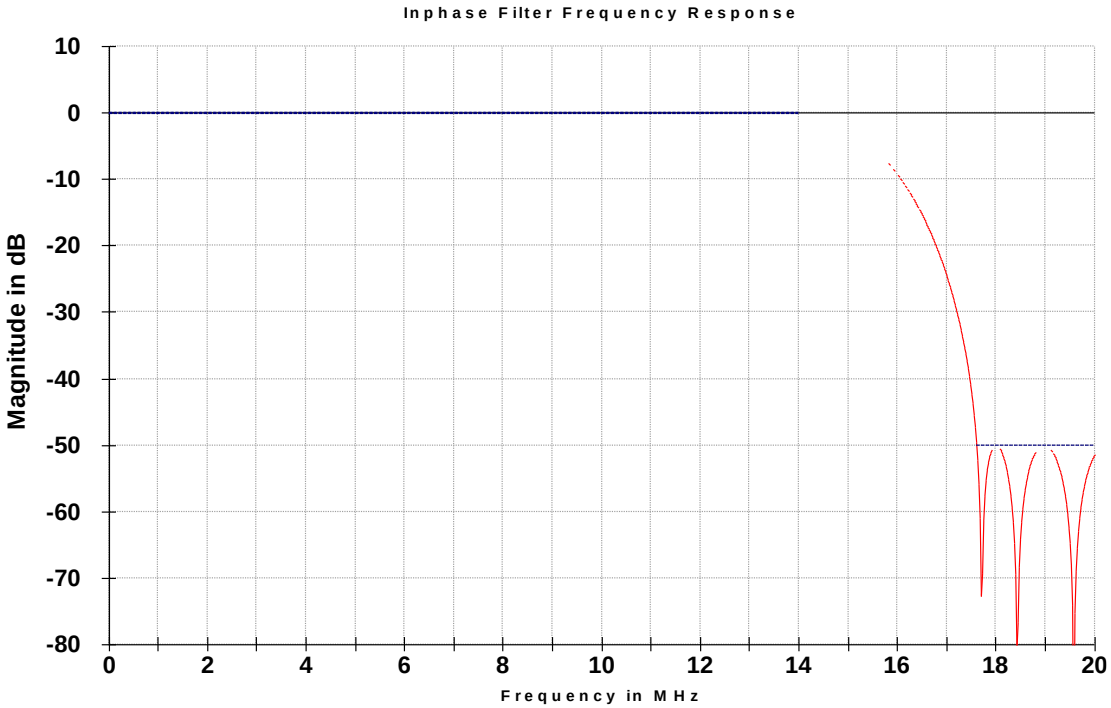

Figure 16 Frequency characteristic of the video demodulation low pass filter.

The sine channel is the demodulated luma (Y) video and the cosine channel is the line-multiplexed chroma (Cb and Cr) video. A SPG module produces a gate pulse which samples the burst sample of the video subcarrier and from it generates an error signal which modifies the video demodulation ratio counter to achieve phase and frequency lock of the video demodulation loop.

Line_delays.v

The Line_delay.v module demultiplexes the chroma channel. The SPG module generates a half horizontal frequency signal. The multiplexed Cb/Cr chroma is the data input to two line stores. For each horizontal one of the line stores is writing and one is reading. For example, if the chroma for the video line is Cb video, this is routed directly through to the Cb output whilst also being written into one of the line stores. On the next line (Cr video) the Cb output is read from the previously written line store. The sequence is the opposite for the Cr output.

Proc_amp.v

The Proc-amp.v (Processing amplifier) module condition the video for the PT52 output. The module applies gain, clipping and blanking to the output signal so that it conforms with the BT1120 output specification. The video outputs are valid on the rising edge of the Clock signal.

8. Data Transfers

TBD.

9. Register interface

Figure 17 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via a 5 bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT52_CSn (chip select) input must be asserted low and the A[4:0] register address and the data for this register set up. The PT52_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT52_CSn input should then be returned high.

For the write to occur reliably the address (A[4:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT52_WRn pulse.

The address input also selects the register data that is presented on the Register_out[7:0] bus. This output is independent of the PT52_CSn or PT52_WRn inputs.

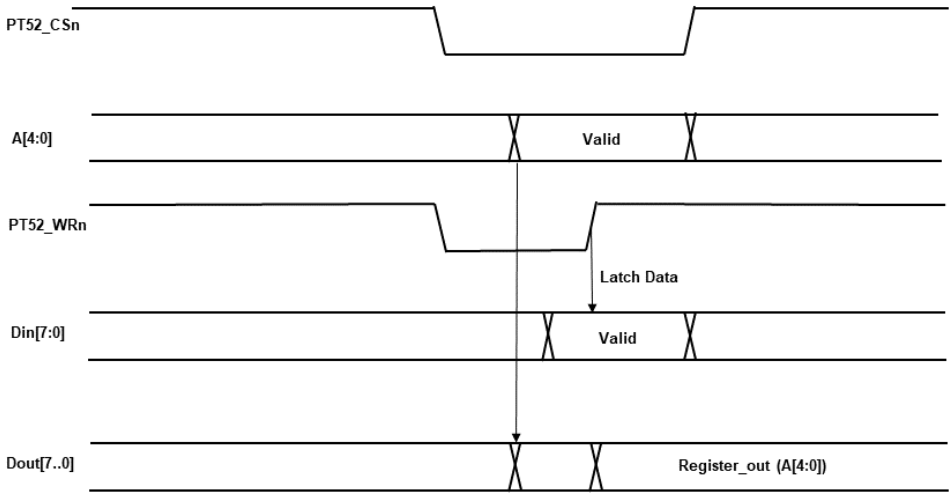

Figure 17 PT52 Register control.

10. Register descriptions

Table 6 lists all the control and status registers. All of the registers are 8-bit; unused register bits read back as zeros.

Please note that some registers can be set to values that are illegal and will produce invalid outputs.

Asserting the RESETn input sets the PT52 registers to their default values.

Register Offset	Register Name	R/W	Bit Value	Description
Control Registers				
Video Input				
Output stage				
Data Transfer				

Table 6 Register Descriptions.