PT54

‘Universal’ Analogue Video Decoder

User Manual

Revision 0.3
26th November 2022

Revision History

Date	Revisions	Version
02-11-2021	First Draft.	0.1
18-01-2022	Evaluation board details updated. FPGA reprogramming information updated. 960p format added.	0.2
26-11-2022	Text corrections. aCVi details added.	0.3

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1. Introduction

PT54 is a 'universal' video decoder IP (intellectual property) core compatible with NTSC/PAL standards, aCVi® and analogue HD formats.

aCVi is a SingMai's proprietary method to transmit high-definition video over long distances (>300m) of low-cost coaxial or twisted-pair cable.

The decoder IP accepts digital composite video at 10-bit resolution which it decodes to a 30-bit YCbCr (4:2:2 format) output with separate horizontal and vertical synchronizing pulses and clock. As standard the PT54 supports the following AHD HD formats: 720p-25Hz/30Hz, 960p/30Hz and 1080p-25Hz/30Hz, 4MP-25Hz/30Hz and 5MP-12.5Hz/20Hz.

Control and status registers are written to and read from using a conventional 8-bit wide microprocessor interface.

The intellectual property block is provided as RTL compliant Verilog-2001 source code for FPGAs from all vendors or for ASICs.

Typical resource usage for an Altera FPGA is shown in Table 1 (as compiled for an EP4CE22 FPGA used on the SM08 PT54 evaluation board).

Logic Cells	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers
11596	189218	26	0	66
24259	189558	26	0	0

Table 1 PT54 Altera FPGA resource requirements

An approximate equivalent for ASIC resource usage is 24259 LCs (logic cell only compile for Altera FPGA) x 14 ~ 340k 2 input NAND gate equivalent.

2. PT54 Module description

The PT54 decoder IP core comprises 21 Verilog modules in a hierarchical structure (see Table 2).

PT54_decoder.v	Register_control.v	
	AA_Filter.v	
	AA_Remod_LUT.v	
	aCVi_Demod.v	
	aCVi_DemodLPF.v	
	aCVi_SPG.v	aCVi_Sync_DemodLPF.v
	vid_nco.v	vid.v
		time_nco.v
		rnd_sat.v
	Demod.v	SinCos_ ROM.v
	DemodLPF.v	
	SPG.v	
	Comb_filter	ram_infer_generic.v
	Delay.v	
	Remod.v	
	Procamp.v	

Table 2 PT54 Verilog file structure.

The top level file is PT54_decoder.v which, in turn, calls 20 of the other modules.

3. Signal Interconnections

The PT54 signal interconnect diagram is shown in Figure 1.

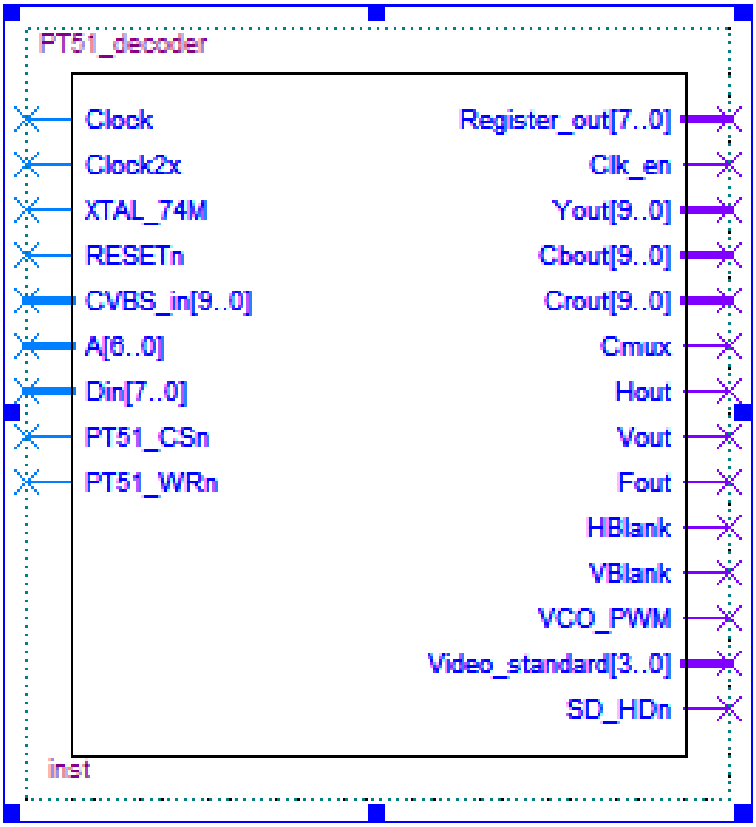

Figure 1 PT54 Block symbol.

The signal descriptions are shown in Table 3, below.

Inputs	
Signal	**Description**
Clock	The clock input from the voltage-controlled oscillator (VCO) or fixed clock source. See Table 4 for the required frequency for the various supported formats. Only the rising edge of this clock is used, so the mark space ratio is not critical.
Clock2x	The 2x clock input from the VCO or fixed clock source. See Table 4 for the required frequency for the various supported formats. This clock is only required for SD video formats. The rising edge of this clock should be aligned with the rising edge of 'Clock'.
XTAL_74M	Fixed 74.25MHz clock used for the automatic standard detection. If this feature is not used this clock is not required and the input may be tied to ground.
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all registers.
CVBS_in[9:0]	Input digital composite video from ADC. Data should be valid on the rising edge of the sample clock. This input should be straight binary (sync tip bottom ~ code '0', peak video white

	~ code ‘1023’).
A[6:0]	Address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT54_CSn	Control chip select input, active low. Used in combination with the WRn input to control writing to the control registers.
PT54_WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers.
Outputs	
Signal	**Description**
Register_out[7..0]	Control output data bus. Outputs the control/status register data selected by the A[6:0] bus.
Clk_en	Clock enable output. All output video and sync signals are valid on the rising edge of Clock when this signal is ‘1’. This signal is nominally at half the frequency of Clock.
Yout[9:0]	Y (luma) output from the encoder. The output is straight binary, blanking level is 64_{10} and peak level nominally 960_{10}. The data output is valid at the rising edge of ‘Clock’ when ‘Clk_en’ is high. Yout[9] is the MSB.
Cbout[9:0]	Cb (B-Y chroma) output from the encoder. The output is offset binary, blanking level is 512_{10}. The data output is valid at the rising edge of ‘Clock’ when ‘Cmux’ and ‘Clk_en’ are high (4:2:2 format). Cbout[9] is the MSB.
Crout[9:0]	Cr (R-Y chroma) output from the encoder. The output is offset binary, blanking level is 512_{10}. The data output is valid at the rising edge of ‘Clock’ when ‘Cmux’ and ‘Clk_en’ are high (4:2:2 format). Crout[9] is the MSB.
Cmux	Data valid output for Cb and Cr outputs. Cb and Cr data is valid on the rising edge of ‘Clock’ when ‘Cmux’ is high (4:2:2 data format).
Hout	Horizontal sync output from decoder (active low). The falling edge of this output is the 0H timing reference (middle of analogue tri-level sync for HD or falling edge of bi-level sync for SD).
Vout	Vertical sync output from decoder (active low). The falling edge of this output is Line 1 of the field.
Fout	Frame sync output from decoder (low for field 1). Only valid during interlaced video formats.
HBlank	Horizontal blanking output from decoder. The duration of this pulse is the active video period of the standard (e.g. 1280 pixels for 720p standards).
VBlank	Vertical blanking output from decoder.
Gain_control	Pulse width modulated output for the control of the analogue input stage voltage-controlled amplifier (AGC). See Chapter 5.
VCO_PWM	Pulse width modulated output for the control of external voltage-controlled oscillator frequency (VCO control voltage). See chapter 6.
Video_standard[3:0]	The selected video standard (or in auto standard mode, the measured video standard). 0000 = NTSC/720p25 0001 = PAL/720p30 0010 = 720p50 0100 = 720p60 0110 = 1080p25

	1000 = 1080p30
SD_HDn	The selected standard definition (SD = '1') or high definition (HD = '0') mode (or in auto standard mode, the measured video standard).

Table 3 PT54 Input/Output signals

The Verilog instantiation of PT54 is shown below:

```
// Instantiate PT54 decoder

PT54_decoder PT54_decoder_inst
(
.Clock(Clock_sig) ,                          // input  Clock_sig
.Clock2x(Clock2x_sig) ,                      // input  Clock2x_sig
.XTAL_74M(XTAL_74M_sig) ,                    // input  XTAL_74M_sig
.RESETn(RESETn_sig) ,                        // input  RESETn_sig
.CVBS_in(CVBS_in_sig) ,                      // input [9:0] CVBS_in_sig
.A(A_sig) ,                                  // input [6:0] A_sig
.Din(Din_sig) ,                              // input [7:0] Din_sig
.PT54_CSn(PT54_CSn_sig) ,                    // input  PT54_CSn_sig
.PT54_WRn(PT54_WRn_sig) ,                    // input  PT54_WRn_sig

.Register_out(Register_out_sig) ,            // output [7:0] Register_out_sig
.Clk_en(Clk_en_sig) ,                        // output  Clk_en_sig
.Yout(Yout_sig) ,                            // output [9:0] Yout_sig
.Cbout(Cbout_sig) ,                          // output [9:0] Cbout_sig
.Crout(Crout_sig) ,                          // output [9:0] Crout_sig
.Cmux(Cmux_sig) ,                            // output  Cmux_sig
.Hout(Hout_sig) ,                            // output  Hout_sig
.Vout(Vout_sig) ,                            // output  Vout_sig
.Fout(Fout_sig) ,                            // output  Fout_sig
.HBlank(HBlank_sig) ,                        // output  HBlank_sig
.VBlank(VBlank_sig) ,                        // output  VBlank_sig
.VCO_PWM(VCO_PWM_sig) ,                      // output  VCO_PWM_sig
.Video_standard(Video_standard_sig) ,        // output [3:0] Video_standard_sig
.SD_HDn(SD_HDn_sig)                          // output  SD_HDn_sig
);
```

Figure 2 shows the interconnections between the PT54 IP core and the voltage-controlled oscillator (if used) and the analogue front end/ADC. The analogue front end/ADC requirements are discussed in detail in chapter 4 and the clock requirements in chapter 5.

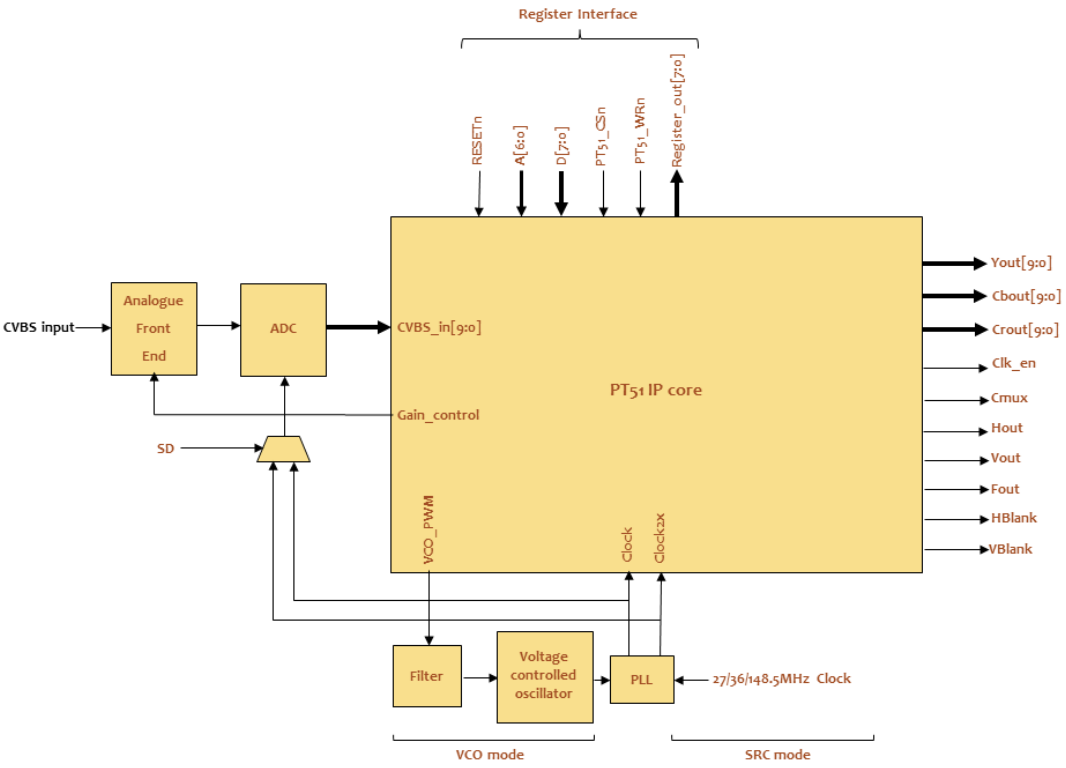

Figure 2 PT54 IP core interconnections.

4. aCVi Overview

The following is a brief overview of the aCVi® revision 2 interface (abbreviated to aCVi® in this document).

aCVi® is a proprietary format, developed by SingMai Electronics, to transmit high-definition video over long distances of coaxial or twisted pair cable. aCVi® is an update to the previous version, specifically designed to interface directly to image sensors, although it may also be used to transmit conventional video sources.

A single chip image sensor, as found in almost all non-broadcast cameras, uses a colour filter to 'assign' each sensor pixel one of red, green or blue sensitivities. Because green is where the human eye is most sensitive, there are twice as many green pixels as red and blue (see Figure 3). This means that if your sensor has a horizontal array of 1920 pixels, only 960 of them are green, red or blue pixels, and for the red and blue pixels, each horizontal line is either red or blue. The actual resolution of the sensor to each colour is for green, 960 x 1080 pixels, and for red and blue, 960 x 540 pixels. (A broadcast camera will use three optically aligned sensors, each offering 1920 x 1080 pixels for the three colours). If we refer to the full resolution (e.g. a broadcast camera) as 4:4:4 sampled, a single image sensor actually produces a 2:2:0 output.

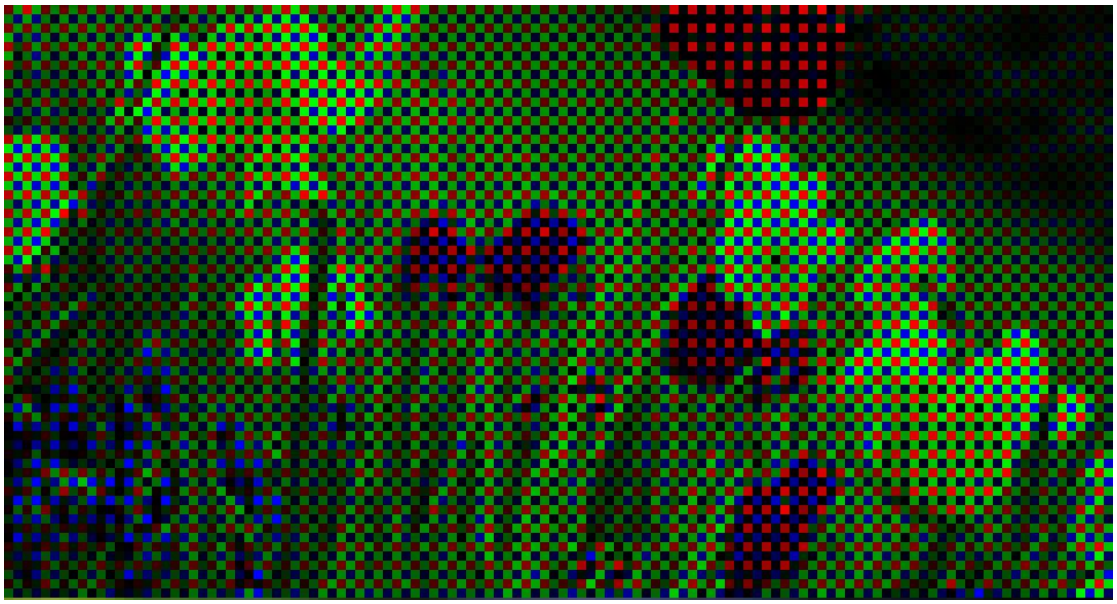

Figure 3 Bayer colour filter.

To conform with video standards (e.g. 1920 x 1080) the additional pixels are interpolated (a technique known as Bayer de-mosaicing) and this function is usually performed in the camera ISP (Image Signal Processor). However, this process can produce artifacts into the image (for example see the colour artifacts on the white fence in Figure 4), and also, because it generates more than double the number of original pixels, more than doubles the bandwidth of the output signal, which exacerbates the problem if the video is required to transmitted long distances.

aCVi® interfaces directly to the single chip image sensor and transmits the RAW 2:2:0 resolution image directly, thereby reducing by more than half the bandwidth of the transmitted signal and achieving higher resolution, lower noise and greater distances.

Figure 4 Left: Original full resolution image. Right: Image after Bayer demosaicing.

aCVi modulates the synchronizing pulses onto one subcarrier (approximately 10.5MHz) and the luma and line-multiplexed chroma (Cb/Cr) onto a separate subcarrier (at approximately 19.5MHz). The spectrum of the aCVi signal is shown in Figure 5. Because there is no DC content to the aCVi video, it is possible to provide DC power upon the same cable. Another advantage, is the use of a proprietary modulation scheme, makes it more difficult for the video to be 'snooped on' and makes it more resilient to external interference.

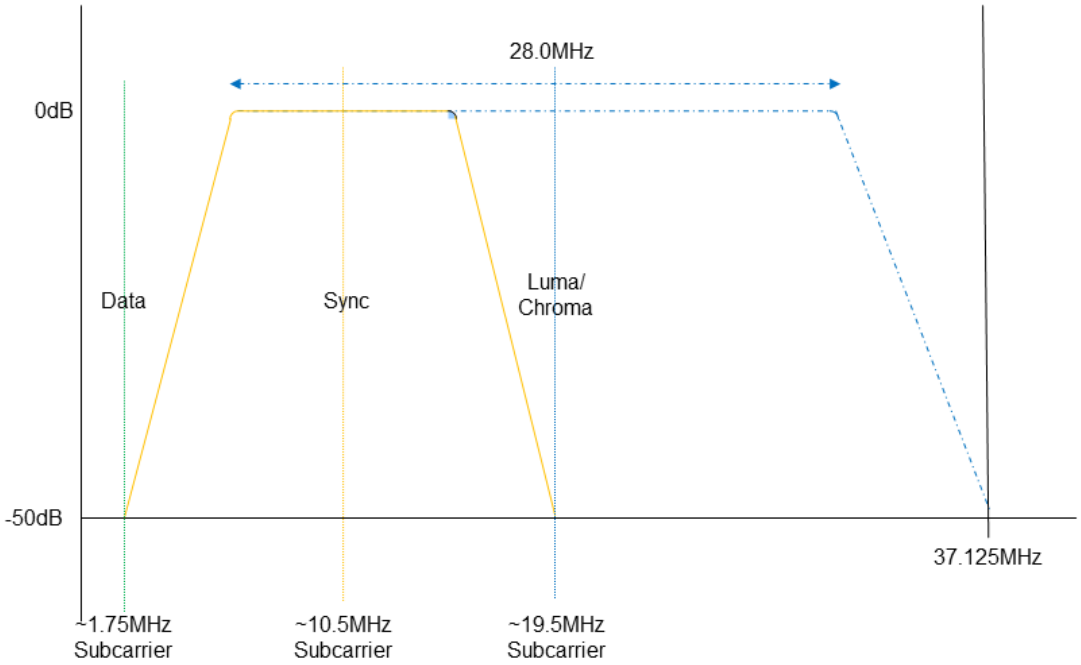

Figure 5 aCVi spectrum.

The available aCVi® IP cores are shown in Figure 6. The PT57 (multi-standard) provides an NTSC/PAL/AHD/aCVi® transmitter for YCbCr (BT1120 style interface) and outputs digital composite video for a digital to analogue converter (DAC).

The receiver IP core is the PT54 (multi-standard). An analogue front end (AFE) conditions the analogue video before it is converted to digital CVBS (composite video) in an analogue to digital converter (ADC). The PT54 decodes the CVBS input into a YCbCr output.

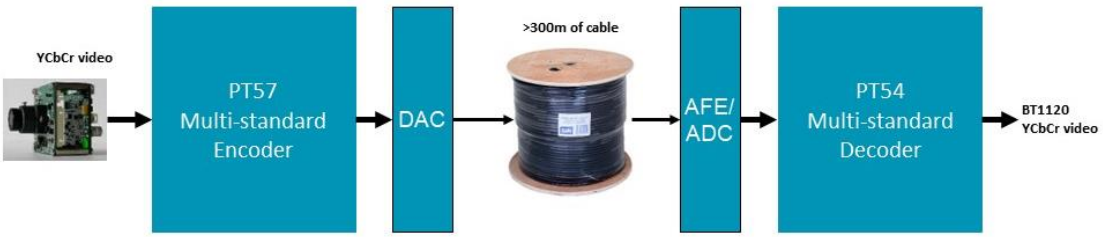

Figure 6 aCVi IP cores.

5. Analogue Front End

Figure 8 shows an analogue front end (AFE) for the PT54. NTSC , PAL and AHD require clamping to restore the DC level of the signal because their average picture level changes, whereas aCVi only requires AC coupling as it has no low frequency content. These two requirements are met in Figure 8.

The board can accept either twisted pair differential inputs (J1) or single ended coaxial inputs (J2). For the latter, the coaxial input has a pseudo-differential input, giving some degree of low frequency noise rejection (for NTSC/PAL/AHD, e.g. hum).

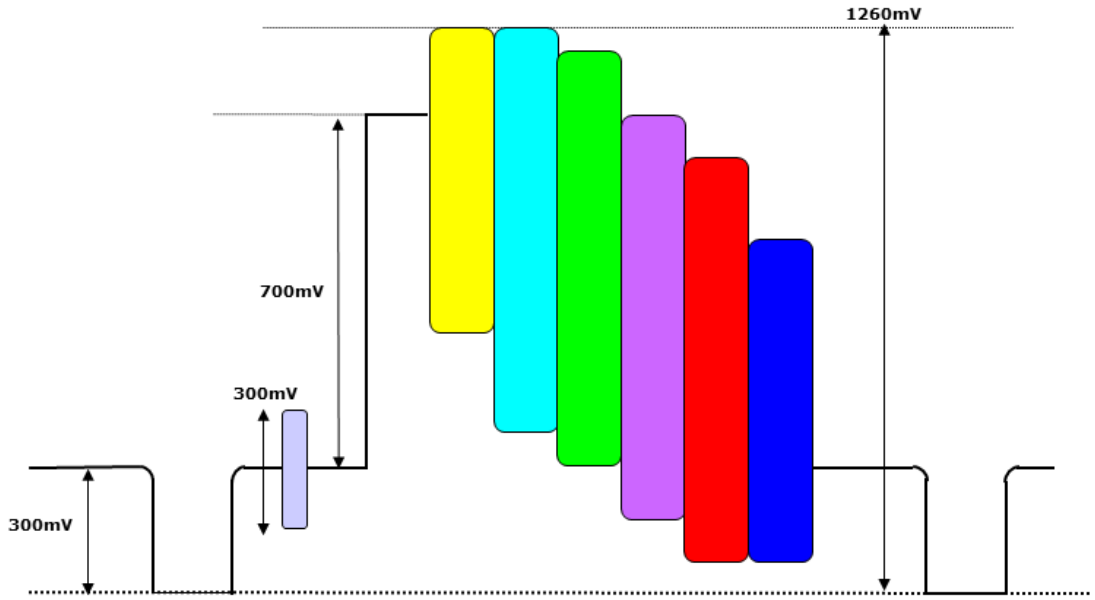

Figure 7 CVBS video input levels.

The typical input voltage levels (for a 100% colour bar input) are shown in Figure 3. The sync, luma and colour modulation depth for AHD are similar to NTSC/PAL. The analogue front end is designed to accommodate a +3dB overhead on this signal to allow over-range inputs without clipping.

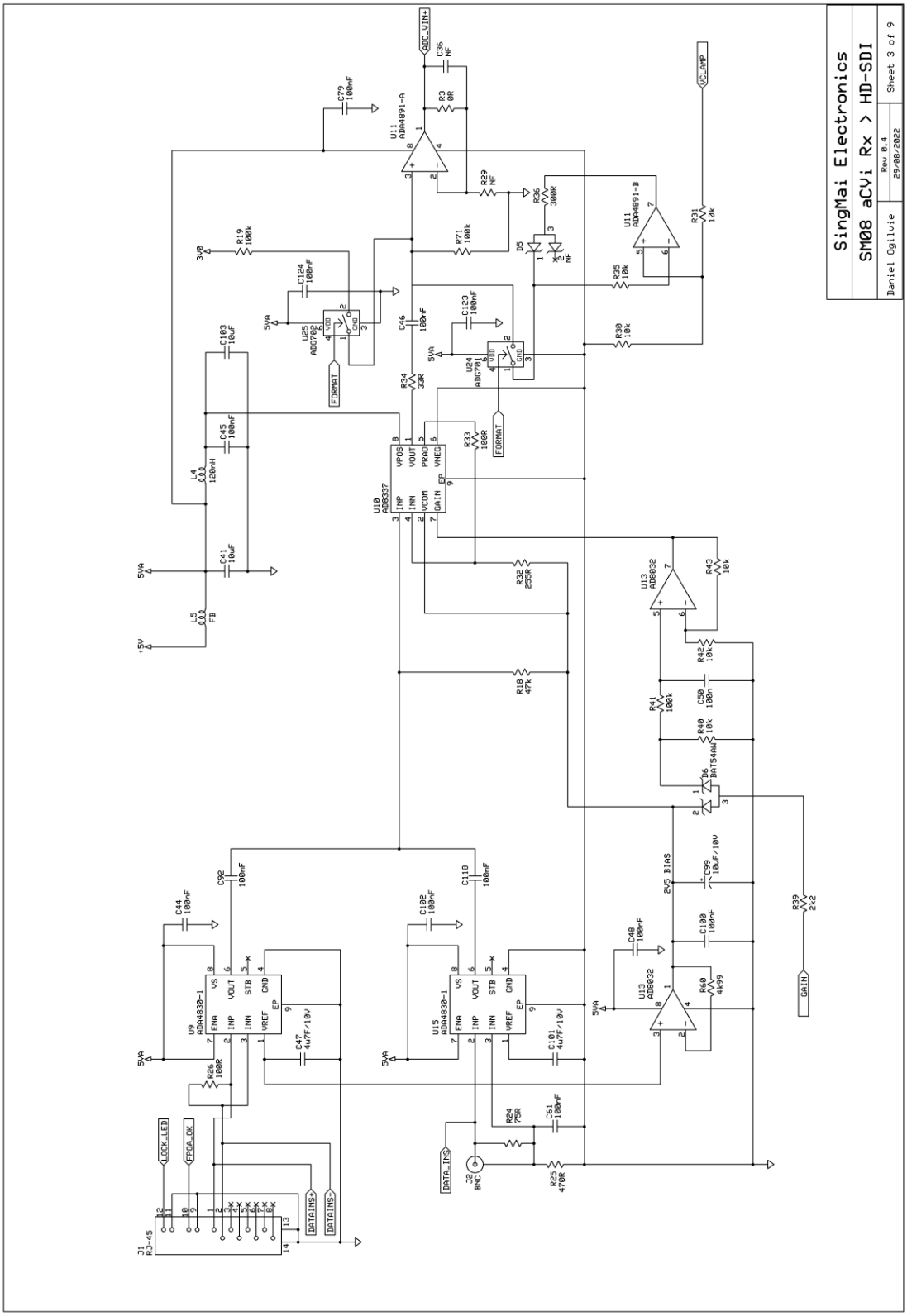

Figure 8 PT54 - Analogue front end schematic.

U9 and U15 convert the (pseudo) differential inputs to a single ended output with a gain of -6dB. U10 is a programmable gain amplifier that is controlled by the PWM input signal, 'Gain_control', which allows compensation for different input levels.

The gain response curve of the AD8337 is shown in Figure 9. The 'Gain_control' PWM output is low pass filtered (by R41 and C50) to convert it to an analogue control voltage. The AD8337 provides a +18dB control range.

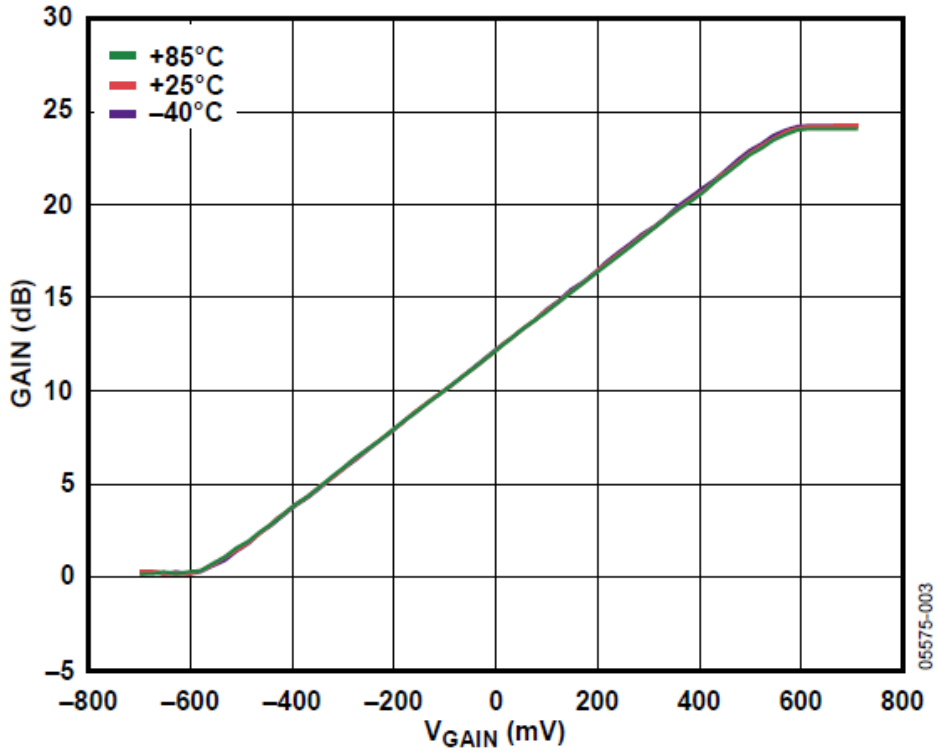

Figure 9 AD8337 PGA gain response.

For non-aCVi inputs the output of the PGA is then clamped to ensure the video signal is scaled through the ADC correctly under large variations in average picture level (APL). The bottom reference of the ADC is used to clamp the most negative part of the input signal, using an ideal diode formed by D5 and U11-B. The black level restoration is performed digitally in the PT54 decoder.

For aCVi the video can just be AC coupled into the ADC with the DC point set at mid-level.

Switching between the two inputs (clamped or otherwise) is performed by analogue switches U24 and U25. The 'FORMAT' control is '0' for aCVi and high for NTSC/PAL/AHD.

The clamped video is then digitized in a dual 10-bit ADC, U19, an AD9216, which is clocked at 148.5MHz for HD video formats and 27MHz for NTSC/PAL (see Figure 10). For 148.5MHz operation the dual ADC is clocked in anti-phase to ease the ADC requirements; for NTSC/PAL a single ADC (ADC A) is used. The output from the ADCs is straight binary coded 10-bit digital CVBS video.

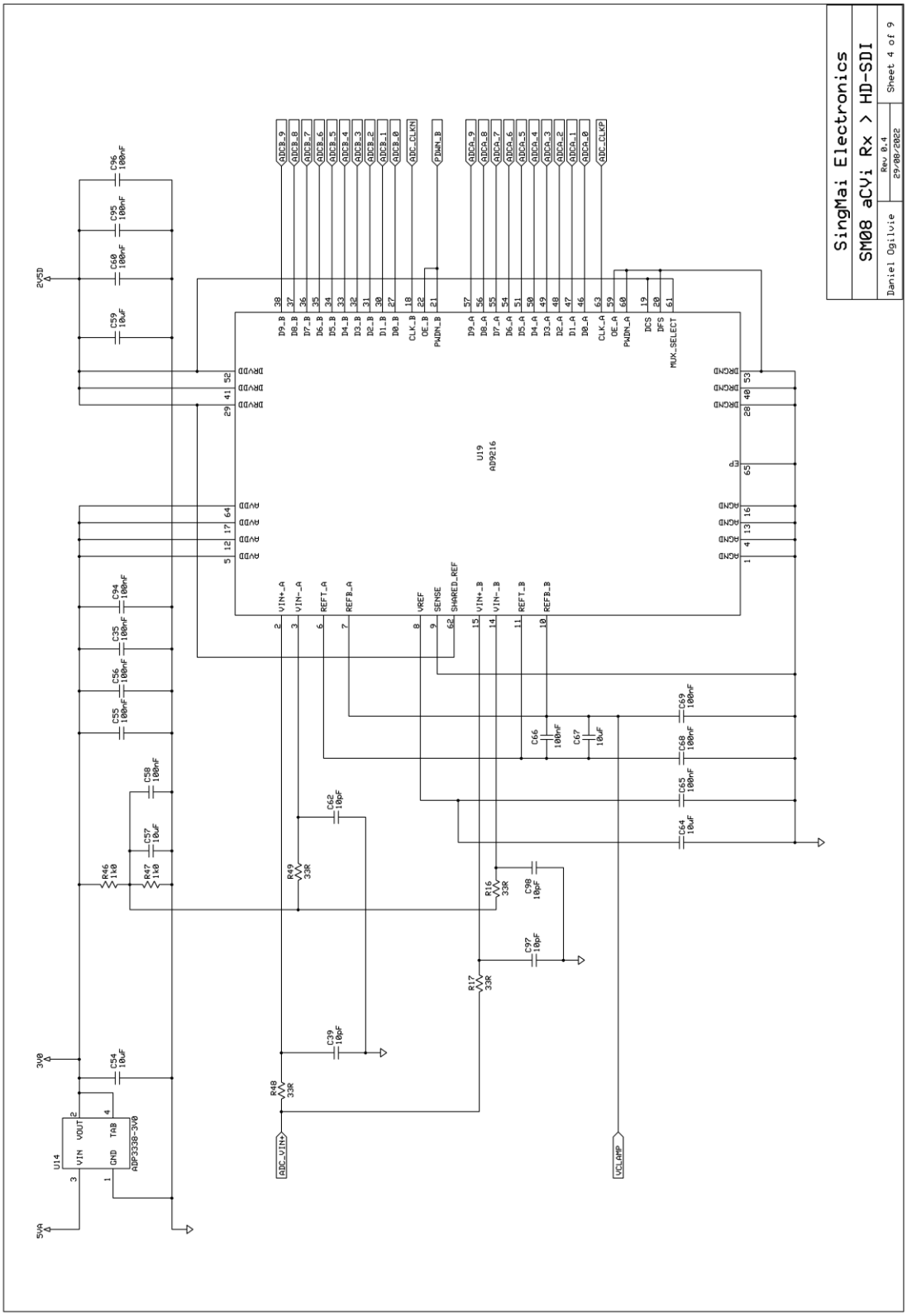

Figure 10 PT54 - ADC schematics.

The peak-to-peak video input range for a 100% modulated PAL colour bar signal is 1.26V. It is prudent to accommodate over-range inputs without clipping so a 2-3dB overhead should be designed for (i.e. 1.26V +3dB = 2.26V): the AFE input stage supply voltage should therefore be >2.5V.

The performance of the complete front end should present no limit to the performance of the PT54. Typically for PAL, the differential gain and phase should <1% and <1°, respectively; the bandwidth should be 5.75MHz ± 0.15dB and the group delay should be <15ns (ideally <10ns). RMS noise from 0 - 5.75MHz should be <-60dB.

6. Synchronisation modes

The clock rates for the supported video standards are shown in Table 4.

Clock	NTSC/PAL	AHD	aCVi	Comments
ADC clock	27MHz	148.5MHz	148.5MHz	For aCVi to support all standards a 148.5MHz/1.001 is required.
PT54 Clock	27MHz	148.5MHz	148.5MHz	For aCVi to support all standards a 74/25MHz/1.001 is required.
PT54 Clock2x	54MHz	NR	NR	Clock2x is not required for AHD or aCVi.

Table 4 PT54 and ADC sample rates.

The PT54 needs to produce a line locked output – that is to say, a video output pixel must appear at the same point in time relative to the horizontal sync pulse. Failure to do so will mean vertical edges will be jagged.
The PT54 provides two methods to produce a line-locked output:

1. The PT54 provides a VCO_PWM output which can be filtered to produce an analogue control voltage to control the frequency of a voltage-controlled oscillator (VCO). This VCO output provides the clock for PT54.
2. The PT54 accepts a fixed clock input frequency and uses sample rate converters and sample dropping to align the video with the clock edge and ensure there are the correct number of samples per horizontal line. A FIFO retimes the output to ensure there is a continuous output without missing samples.

The PT54 SPG module extracts the horizontal sync signals from the composite CVBS inputs. The SPG module also divides the 'Clock' input to produce a signal at the same approximate frequency as the horizontal line pulse. For example, for AHD 720p/60Hz, dividing the 74.25MHz clock by 1650 (the number of pixels/line according to the video standard) produces 45kHz, the line frequency of the 720p/60Hz standard. The SPG module then compares the phase of this 45kHz signal and the recovered horizontal sync signal. The error in phase is then used to adjust the frequency of the 'Clock' input such that the two falling edges of the horizontal sync signals align. When this occurs the horizontal input sync and the Clock will be in phase and we will have a line-locked output.

In synchronizing mode 1 (VCO mode) the phase error word generated in the SPG module is converted to a pulse width modulated (PWM) which is converted to analogue voltage to control the frequency of the VCO. The external VCO circuit used in the PT54 evaluation board (SM08) is shown in figure 6.

The PWM signal is low pass filtered (R11 and C32) and buffered (U7), to become the analogue control voltage to a VCXO (voltage-controlled crystal oscillator). The frequency output of this oscillator should comply with the requirements shown in Table 4. In addition, for SD standards (the anti-aliasing filter and the line delays for the comb filter require it), a twice clock frequency input to the PT54 is required (Clock2x). The rising edges of Clock and Clock2x should be aligned.

In lock mode 1, the sample rate converters are set to bypass by setting Control register 3, bit 6 to '1'. The SRC will then produce a fixed half frequency clock enable output that is used to gate all subsequent registers. For example, for NTSC/PAL, the video and input clock to the sample rate converter (SRC) is 27MHz. All subsequent registers are also clocked at 27MHz but enabled using the Clk_en output of the SRC, which is at 13.5MHz. Effectively the PT54 is running at 13.5MHz.

A VCXO (Voltage Controlled Crystal Oscillator) is used on the SM08 PT54 evaluation board. However, any oscillator may be used that meets the stability requirement. The 'pull' range of VCXO is limited, which means that some out-of-range NTSC/PAL inputs cannot be locked to because we cannot adjust

the frequency of the VCXO more than ±150ppm (±0.15%). To accommodate all NTSC/PAL signal sources, including mechanically scanned sources such as VCR or laserdisc, a pull range of ±7% should be designed for.

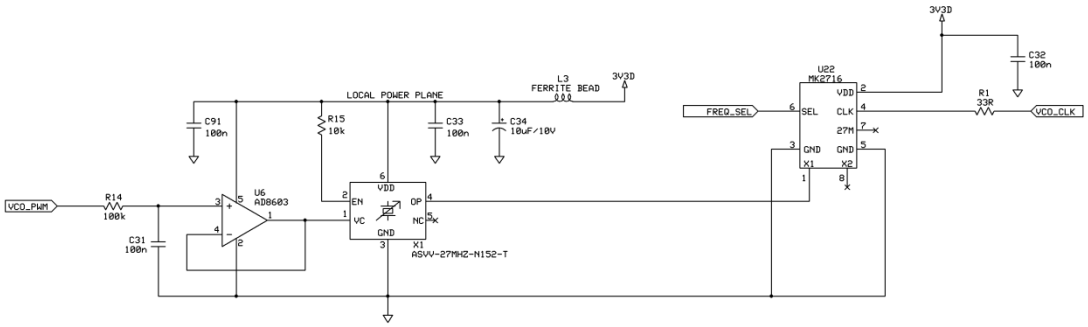

Figure 11 External VCO schematic.

For the comb filter to separate the chroma and luma properly, and to reduce the jitter on the chroma vectors to less than 1° (the broadcast NTSC/PAL specification), the clock jitter should be less than 1/(4.4335MHz [PAL subcarrier frequency] x 360) = 626ps. This is the short-term jitter, which for the comb filter requirement is 2/15.625kHz = 128µs (the aperture of the PAL comb filter is 2 horizontal lines/field): i.e. the short term (128µs) peak jitter of the VCO should be <0.6ns.

In lock mode 2, the PT54 only requires a fixed clock input. If both lock modes are required Control, register 3, bits 5:4 can be set to '11' which sets a 50% duty cycle output to the VCO_PWM output to adjust the VCO to its mid-point frequency range.
The horizontal phase error is generated in the same way as for lock mode 1. However, the phase error word is instead used to adjust the phase of the video input instead of the clock. This is achieved by using a Farrow filter structure in the SRC. The SRC can be thought of as a multi-phase filter which, by selected appropriate taps allow us the alter the phase of the output video over a ±0.5 pixel range. If the input video is more than ±0.5 pixels in error from our generated horizontal clock, then the Clk-en (clock enable) can add or subtract cycles of the clock to effectively produce a coarse phase adjustment. Under this condition the video output may not be continuous.

Figure 13, upper, shows the continuous output video when in lock mode 1. In this mode we adjust the frequency the clock, so although the 13.5MHz nominal output may be slightly more or less than this, the video output is continuous.
In lock mode 2, the Clk_en output may not be at a fixed half frequency and the output may produce two cycles of video data at 27MHz, or no new video data for a clock period (see the bottom waveforms of Figure 13). To avoid this non-continuous output a FIFO is used to re-time the output.

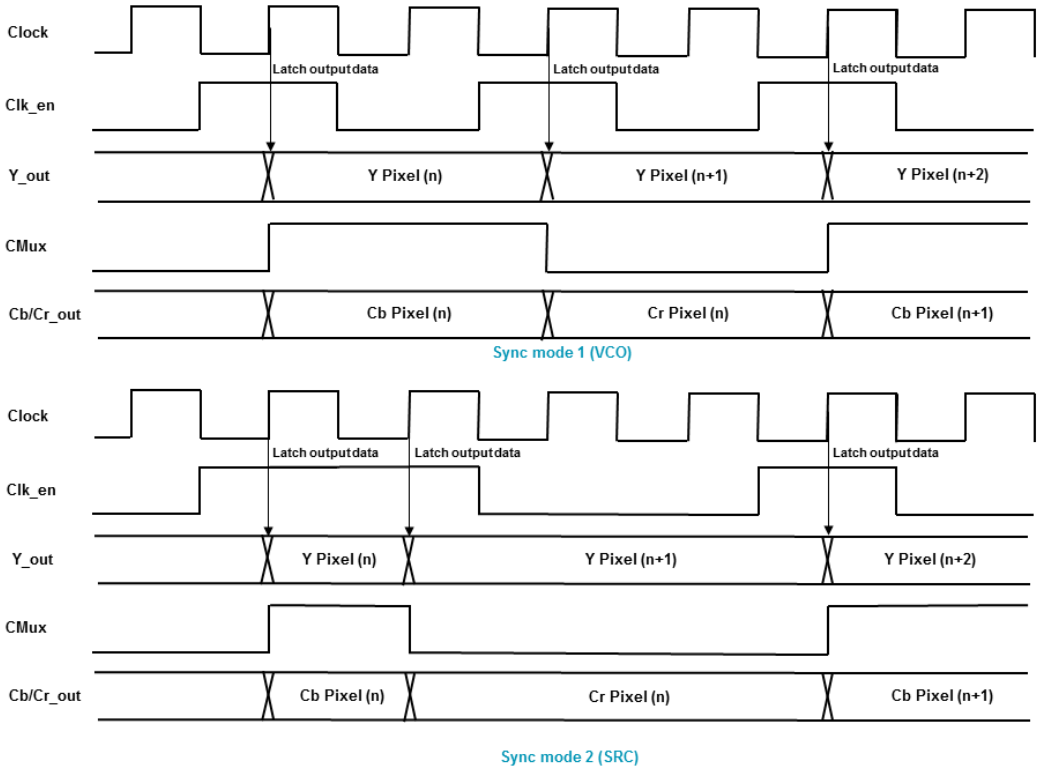

Figure 12 PT54 lock modes: Output Timing.

7. Technical Overview

A simplified block diagram of the NTSC/PAL/AHD decoder is shown in Figures 13 and 14. The front end of the video decoder is clocked using the 'Clock' input (e.g. 27MHz for SD video or 148.5MHz for HD video).

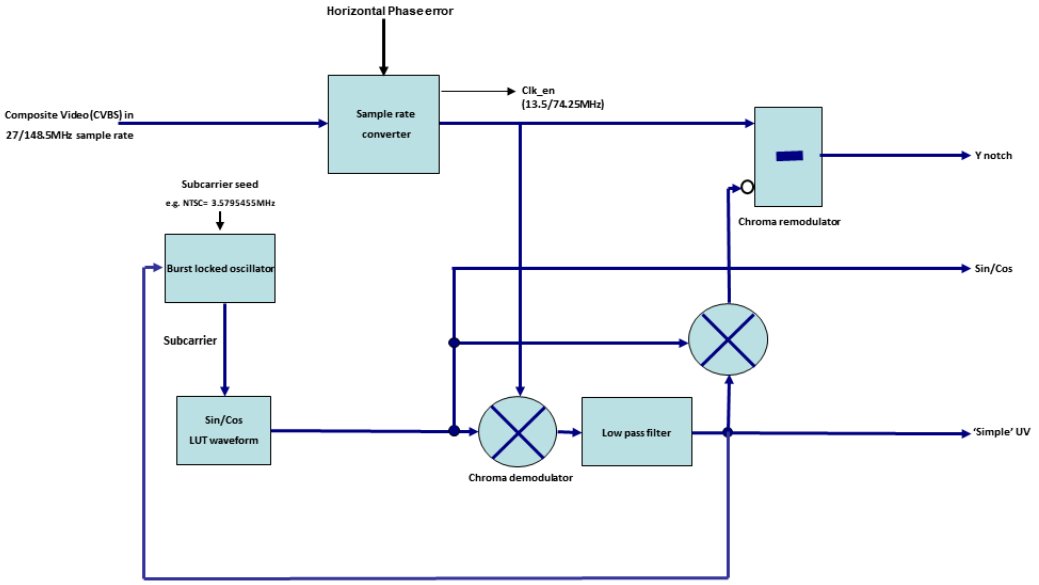

Figure 13 PT54 Block diagram - Front end.

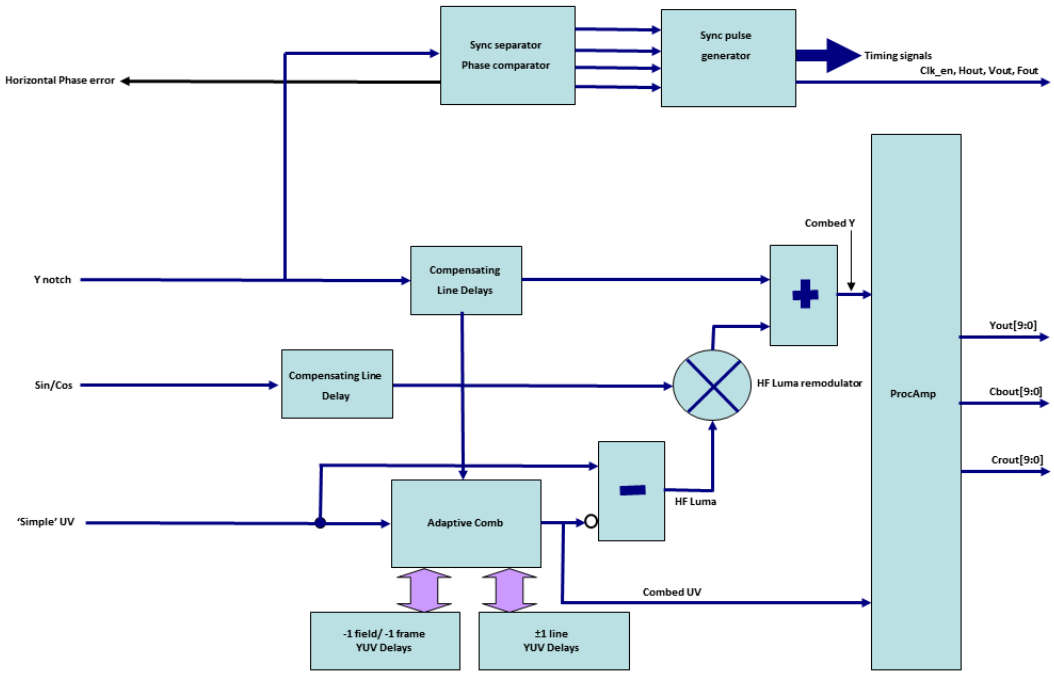

Figure 14 PT54 Block diagram - Back end.

The input from the ADC is straight binary coded at 10-bit resolution. The supported standards are shown in Table 5.

Format	Pixels/line	Active pixels/ line	Line frequency	Lines/ frame	Active lines/ frame
NTSC-M	858	720	15.734kHz	525	484
PAL	864	720	15.625kHz	625	576
720p/25Hz AHD	1980	1280	18.75kHz	750	720
720p/30Hz AHD	1650	1280	22.5kHz	750	720
960p/30Hz AHD	1400	1280	33.75kHz	1125	960
1080p/25Hz AHD	2640	1920	28.125kHz	1125	1080
1080p/30Hz AHD	2200	1920	33.750kHz	1125	1080
1440p/25Hz AHD (4M25)	3960	2560	37.5kHz	1500	1440
1440p/30Hz AHD (4M30)	3300	2560	45.0kHz	1500	1440
1944p/12.5Hz AHD (5M12.5)	3000	2592	24.75kHz	1980	1944
1944p/20Hz AHD (5M20)	3750	2592	39.6kHz	1980	1944

Table 5 NTSC/PAL/AHD formats.

Analogue clamping prior to the ADC ensures the most negative value of the input signal (the sync tips) are clamped to the negative reference of the ADC (code value '0').

The following is a brief description of each Verilog module.

6.1 PT54_decoder.v

This is the top-level module for the PT54. It provides the interconnection between all the other modules.

6.2 Register_control.v

A conventional 8-bit microprocessor style control is used to write and read to the PT54 control registers. Details of the interface may be found in Chapter 7 and the register descriptions may be found in Chapter 8.

6.3 Vid_nco.v

The composite video from the ADC is sample rate converted (in lock mode 2 – in lock mode 1 the sample rate converter is bypassed [Control Register 3, bit 6]).

Vid_nco.v and its three sub-modules, time_nco.v, vid.v and rnd_sat.v form a video sample rate converter.

In lock mode [2] the front end is running at a fixed clock rate of 27MHz (for SD video) or 148.5MHz for HD video. The sample rate converter clocks a ratio counter at 'Clock' frequency and provides an enable output at half this rate (on average) which is used to gate the clock of the decoder.

The ratio counter is adjusted by adding/subtracting a phase error signal – generated by the horizontal phase detector in the SPG.v module – to the seed value.
The ratio counter also provides a phase word which is used to interpolate the 'mid-point' of the video samples and map the incoming video onto the new clock domain. The video interpolator can adjust the video by ±0.5 pixels – more adjustment is provided by dropping or adding clock cycles via the enable signal.

The interpolator uses a Farrow structure; the output from the sample rate converter is an approximate half-clock enable signal (Clk_en) and the interpolated composite video.

6.4 Demod.v

A free-running subcarrier frequency is generated using a 32-bit ratio counter clocked from the input clock.

$$ratio = \frac{\text{phase change per line}}{\text{pixels per line}} = \frac{F_{sc}}{\text{Clock frequency}} = \frac{\Delta\theta_{sc}}{360°} = \frac{\text{subcarrier seed}}{2^{32}}$$

The top 11 bits of this ratio counter (the phase word) are used by the demodulator to generate the sine and cosine waveforms.

For the demodulation to correctly operate the generated subcarrier must be frequency and phase locked to the CVBS video subcarrier which is done by measuring the amplitude of the demodulated and low pass filtered V output during the colour burst. If the frequency and phase of the free-running subcarrier and the colour burst are the same, then this error will be zero. The reference for the BLO is the demodulated and filtered V output from the demodulator low pass filter; 32 samples of this waveform are taken during the burst pulse (16 for NTSC/PAL); the burst gate pulse from the SPG is used for this purpose.

The seed word is modified using the phase error signal until the input colour burst and the ratio counter are phase locked.

The lower 9 bits of the 11-bit phase output from the BLO (burst locked oscillator) are used to address a sine and cosine lookup table (SinCos.v). These 9 bits comprise the phase angle, at subcarrier frequency, within a single quadrant and the top two bits are the quadrant – this method saves memory by only requiring a single quadrant of sin and cos values to be stored in the LUT. The output of the Sin/Cos LUT is a 24 bit word; 12 bits cosine and 12 bits sine. The quadrant signs are used to manipulate the sine and cosine data such as to construct a full waveform.

The reconstructed sine and cosine waveforms are then multiplied by the input CVBS composite video from the ADC. The output of the sine channel is the demodulated U signal and the cosine channel is the demodulated V output. One over-range bit allows for twice subcarrier frequency components (removed by the subsequent low pass filter).

The Demod.v module also measures the amplitude of the demodulated U and V channels. The amplitude of the V channel is used to determine if the BLO has achieved lock. The amplitude of the U channel is used to measure the burst amplitude for the HF boost compensation.

6.5 DemodLPF.v

The output of the demodulator also comprises twice subcarrier frequencies which are removed using a 47-tap low pass FIR filter, the responses for which, for the different standards, are shown in Figures 15-17.

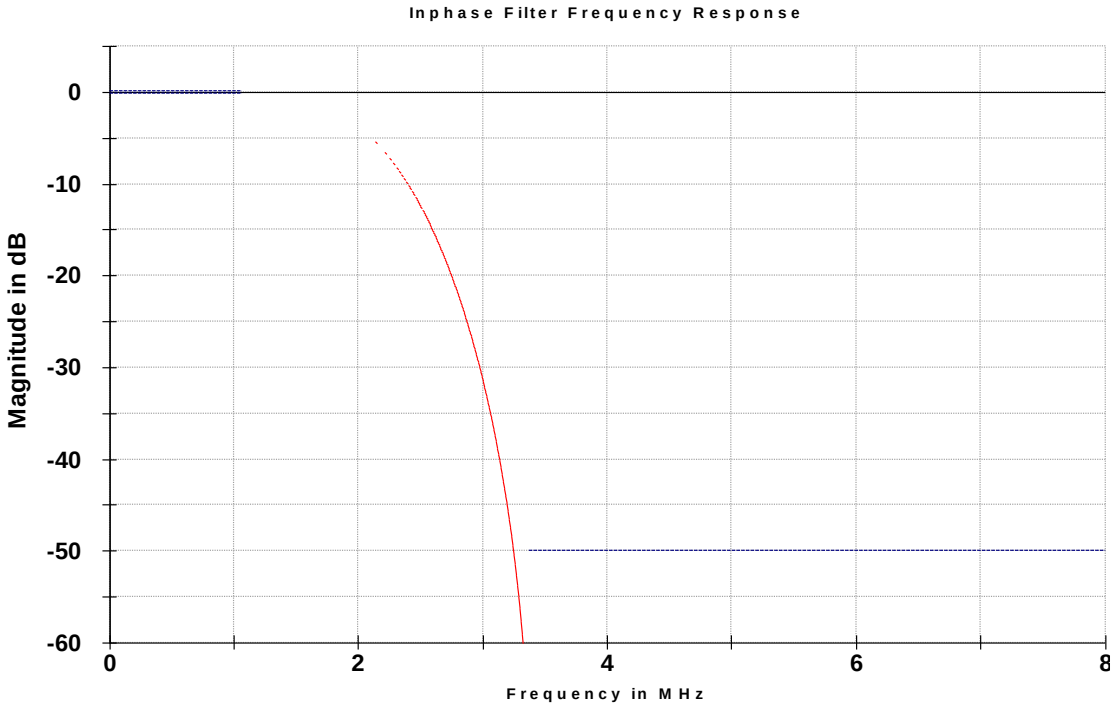

Figure 15 Chroma demodulator low pass filter (NTSC/PAL standards).

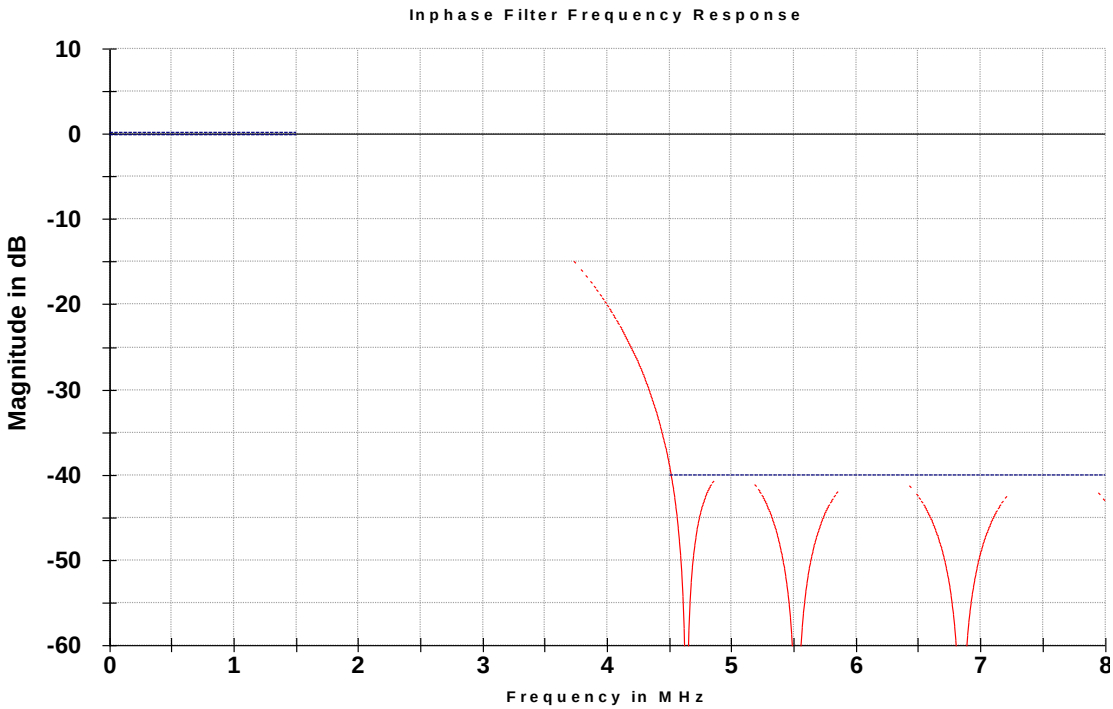

Figure 16 Chroma demodulator low pass filter (AHD 720p).

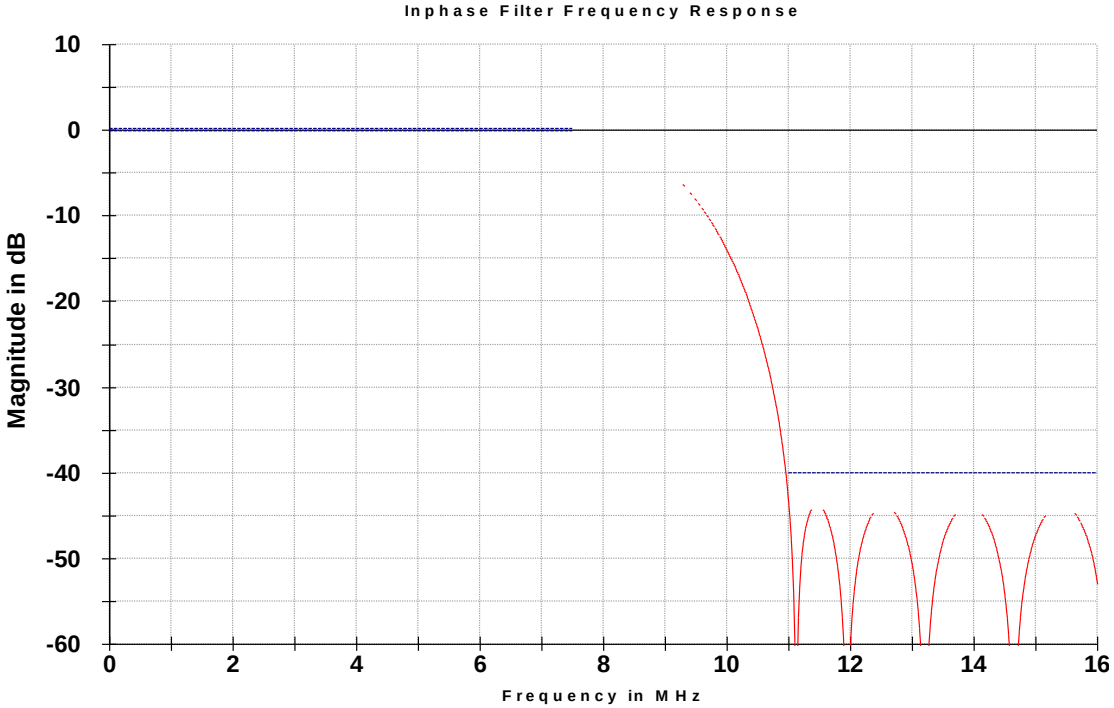

Figure 17 Chroma demodulator low pass filter (AHD 1080p).

6.6 Delay.v

For SD formats the CVBS, Sin and Cos waveforms are passed through a compensating delay (to compensate for the demodulation low pass filters). For HD formats the CVBS video is low pass filtered to remove the chroma component. The filter is a 47-tap FIR filter. The response of the filter for the various formats are shown below.

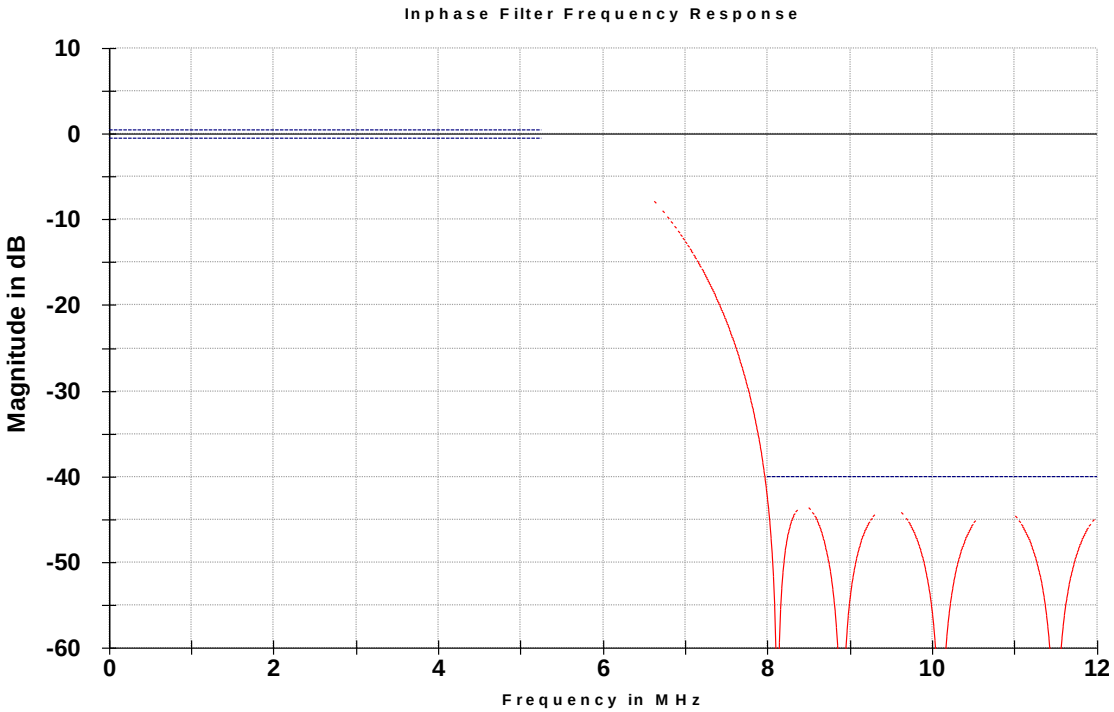

Figure 18 Luma low pass filter (AHD 720p).

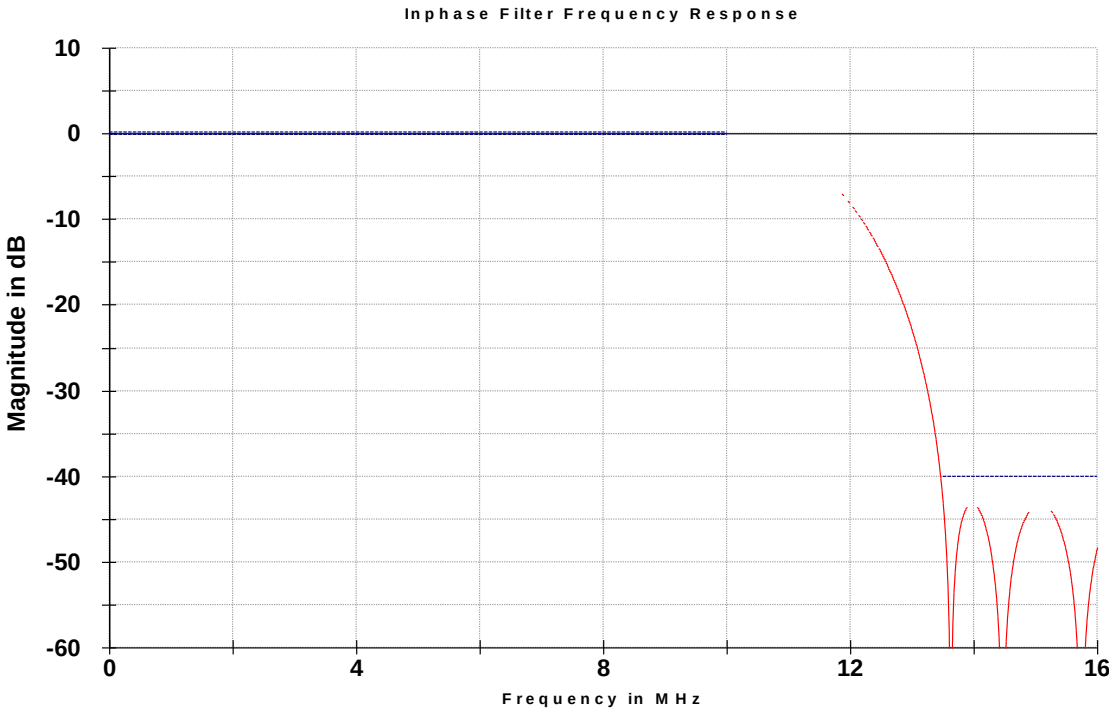

Figure 19 Luma low pass filter (AHD 1080p).

6.7 Comb_filter.v

The demodulated 'simple' U and V outputs also contain high frequency luma information, (cross colour). This can removed for NTSC and PAL standards as the chroma information has a known line based phase relationship whereas the HF luma and cross colour does not. The comb filter provides this filtering operation.

The comb filter is a chrominance comb in that it reinforced the chroma signals whilst cancelling the cross-colour components.

The 3D comb filter (using external memory) is an asymmetric frame comb which provides for minimum latency through the decoder (less than 100µs).

The frame comb filter for NTSC is 1/2*0F + 1/2*1F (1 frame spacing) and for PAL 1/2*0F + 1/2*2F (2 frame spacing). The field comb filter for NTSC is 1/2*0F + 1/2*1F (262 line spacing) and for PAL 1/2*0F + 1/2*1F (312 line spacing).

The line comb filter for NTSC is (1/4*1H + 1/2*2H + 1/4*3H) (1 line spacing) and for PAL (1/4*0H + 1/2*2H + 1/4*4H).

The notch filter mode reduces the bandwidth of the chroma output, thereby reducing cross-colour amplitude. A simple ¼, ½, ¼ filter is used with a spacing of 4 clocks at 13.5MHz.

The zone plate images for each of the PT5 comb filter modes are shown in Figures 20-22.

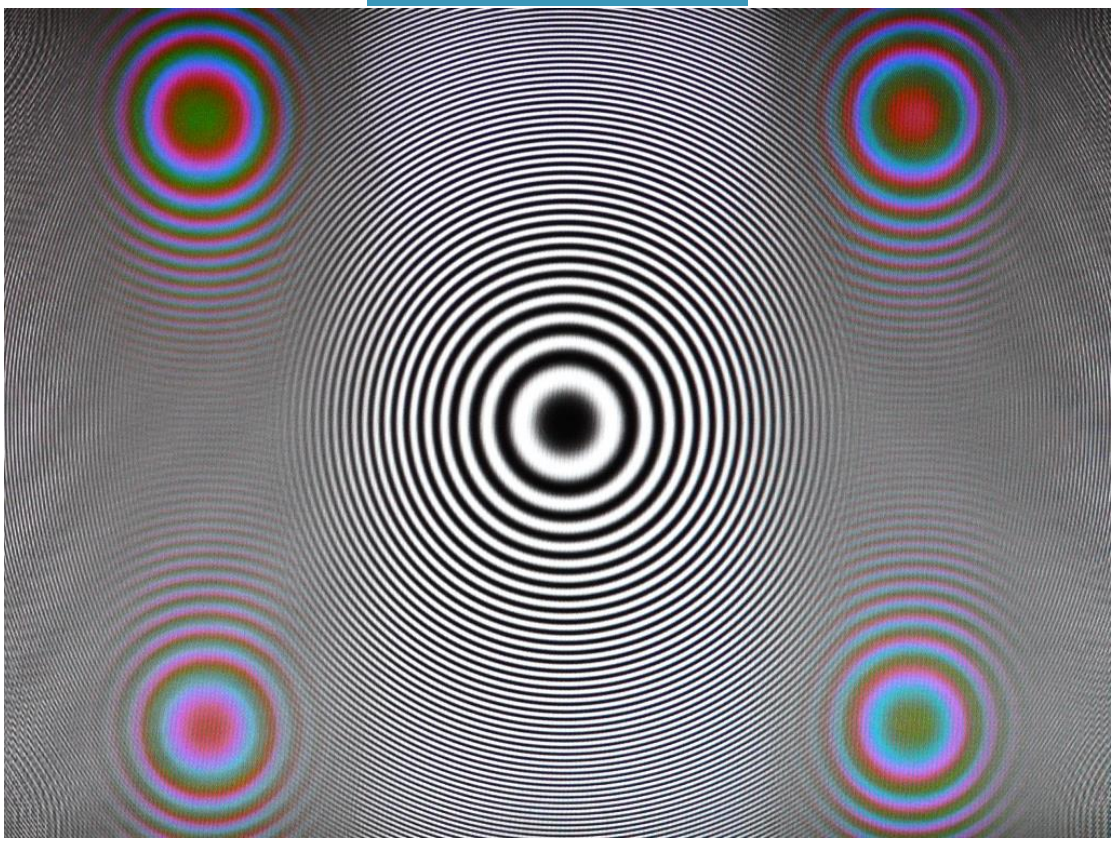

Figure 20 Zone plate: Notch filter

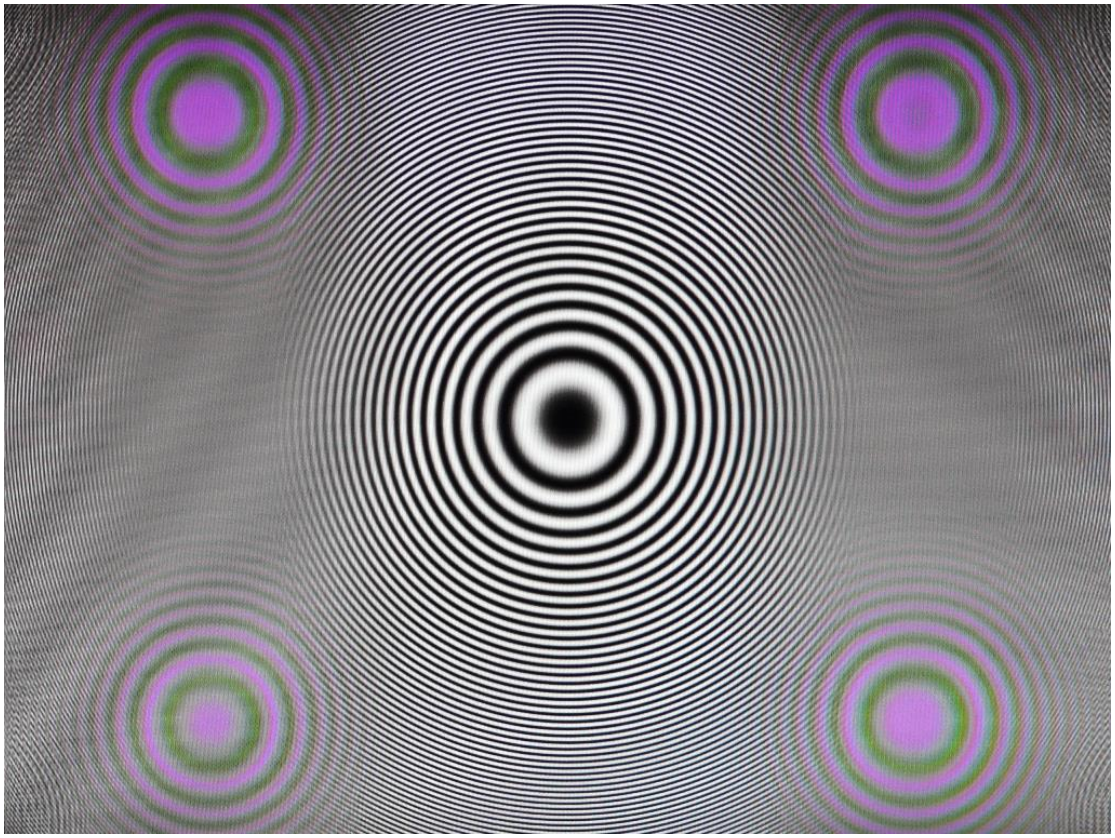

Figure 21 Zone Plate: Line comb

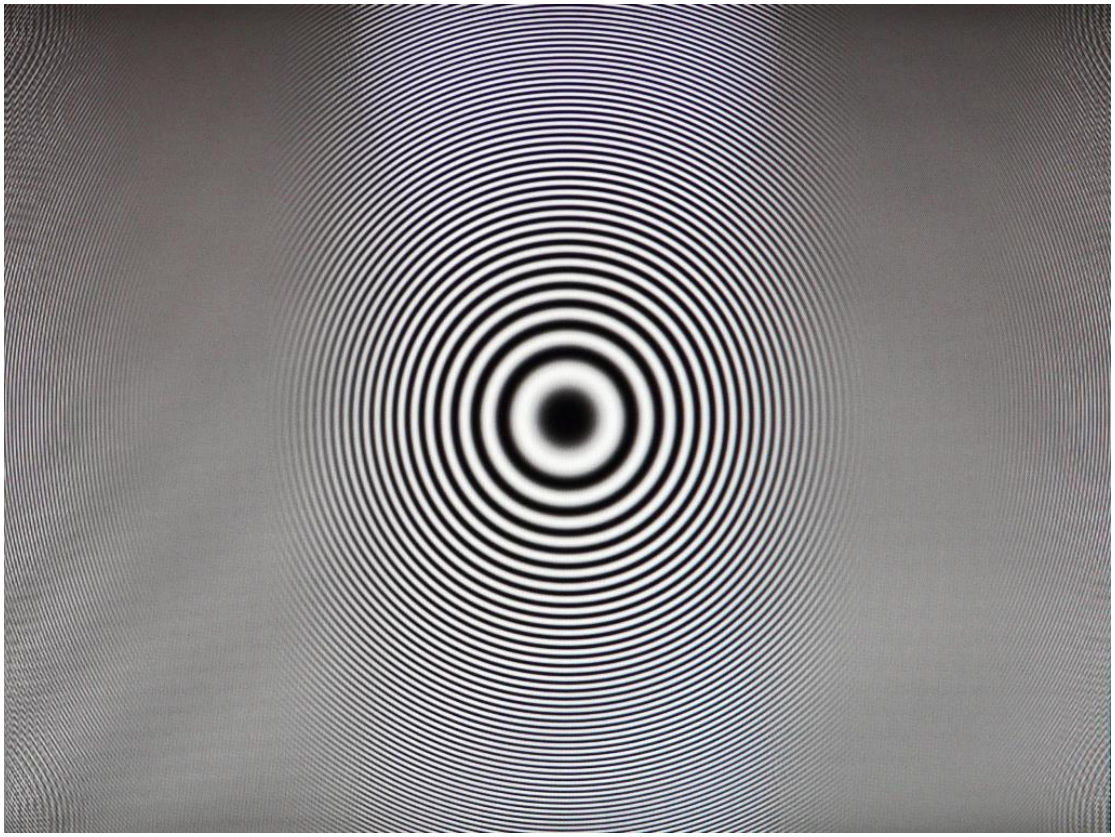

Figure 22 Zone Plate: Frame comb

For the comb filters to operate correctly the phase relationship of the colour component must be maintained. If not the HF luma will not be cancelled and can even be reinforced. It is therefore necessary to detect when the comb filters fail and switch to a better mode.
A diagram illustrating why this occurs across two lines of the composite input is shown in Figure 23.

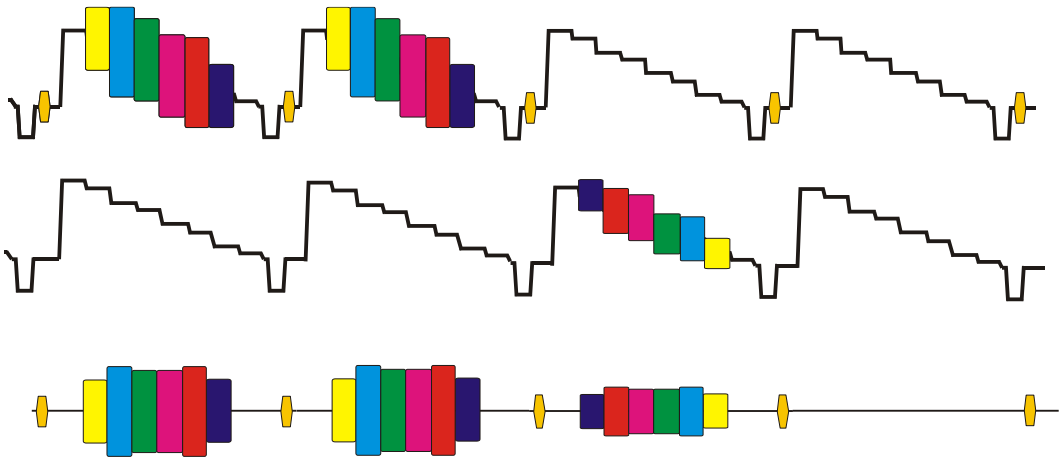

Figure 23 NTSC comb failure

Normally this failure mode is detected using luminance differences across the comb taps but there are instances where the same luminance value can occur but there are different chroma values which still cause the comb to fail. **The PT5 comb adaptation detects value differences in luma, U and V comb taps thereby detecting all comb failure instances.**

The failure value of each comb mode (including notch mode) is compared and the lowest error mode selected on a pixel by pixel basis.

The chosen U and V outputs from the filter are input to the processing amplifier. If the U and V outputs of the comb filter is subtracted from the delayed 'simple' U and V inputs to the comb (delayed by the comb filter delay) the output will be the recovered high frequency luma. This high frequency luminance signal is then sent to the HF luma module to be added to the notched luma.

6.8 3D comb filter memory requirements

The 3D comb filter can provide near perfect, artefact free decoding: (I say near perfect because frame combs are very sensitive to clock jitter and peak to peak clock jitter as little as 0.6ns over the frame delay period can result in residual subcarrier. PAL also has an additional subcarrier offset of 25Hz which means perfect cancellation cannot occur even with a frame comb).

The 3D comb filter is an asymmetrical field and frame comb i.e. one field delay and one frame delay (or two frame delays for PAL) are required. One write port and two read ports are required.

The output to the 3D comb is a 30 bit data bus, 10 bits of Y, Cb and Cr (Y_comb_delay_out[9:0], U_comb_delay_out[9:0], V_comb_delay_out[9:0]. The data is valid on the rising edge of the Clock when the Clk_en output is high.
The inputs from the comb filter delay are also 30 bits, one for the field delay (Y_fieldcomb[9:0], U_fieldcomb[9:0], V_fieldcomb1[9:0]) and one for the frame delay (Y_framecomb[9:0], U_framecomb[9:0], V_framecomb[9:0]).

The field delay requires an exact delay of ((262 lines x 858 pixels) – 6 pixels) for NTSC and ((312 lines x 864 pixels) – 6 pixels) for PAL.

The frame delay requires an exact delay of ((525 lines x 858 pixels) – 6 pixels) for NTSC and ((1250 lines x 864 pixels) – 6 pixels) for PAL. The frame delay tap also allows us provide 3D luma noise reduction.

The S625_525n output from the PT54 can be used to select the delay. The 6-pixel offset is to allow for the comb signal processing in the PT54.

6.9 Remod.v

The combed U and V components are then frequency shifted back to the subcarrier frequency using the delayed sine and cosine waveforms from the Demod.v module, added together to create a chroma component (which in line comb module will contain no high frequency luma information) and subtracted from the composite video to form a 'clean' luma signal. The complementary nature of this architecture ensures there is no missing information from the final luma output. The Remod.v module is bypassed in HD mode.

6.10 SPG.v

A fixed offset is subtracted from the CVBS video such that the midpoint of the sync pulse is at value 0. The horizontal counter addresses a look up table whose output coefficients form a FIR low pass filter to remove chroma composite video. The coefficients are multiplied by the offset video and accumulated across the aperture of the filter, being updated once per horizontal line. The frequency response of the phase detector filter is shown in Figure 16.

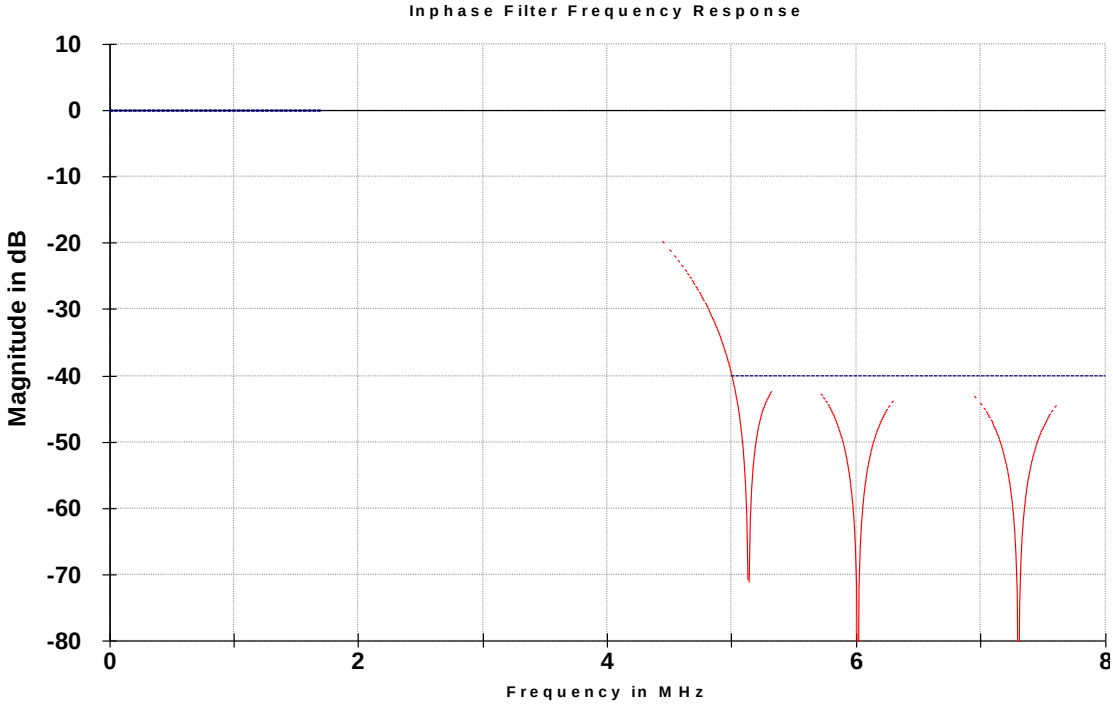

Figure 24 Phase detector low pass filter response.

When the midpoint of the falling edge of the horizontal pulse is coincident with the centre tap of the FIR filter the accumulated result will be zero. When they are not coincident an error will be generated. This error is filtered using a recursive filter (integrator) and proportional and integral terms are added to create an error word which is converted to a PWM signal to control an external voltage-controlled oscillator (VCO).

The horizontal pixel counter is used by the SPG, (sync pulse generator), to provide the horizontal timing pulses required by the decoder, including the burst gate pulse for the demodulator, which must lie in the centre of the colour burst signal.

The vertical field pulses are recovered by using a digital integrator on the sliced filtered video. The SPG also provides Vout (vertical field), Fout (frame ID for interlaced video) and Hout (horizontal) synchronizing pulses.

The SPG also detects the input video standard. The number of field pulses/second, the number of lines/field, whether interlace is detected and the number of pixels/line are all used to determine the input standard. The resulting default values for each standard are then automatically loaded into the appropriate registers (in auto-register mode).

6.11 Procamp.v

The outputs of the sample rate converters are conditioned by the processing amplifier. First the black level offset of the luma (measured in the SPG module) is subtracted from the luma signal to set the black level at zero. The luma is then offset (to 64 code) and amplified to provide a 960 code (10 bit) output for a 75/100% colour bar input.

The low pass filtered chroma outputs are amplified separately to provide a nominal $\pm 262.5_{10}$ code output for a 75% colour bar input. The Cb and Cr outputs are offset binary, with the blanking level at 512_{10}.

6.12 aCVi decoder

The block diagram of the PT54 aCVi decoder is shown in Figure 25.

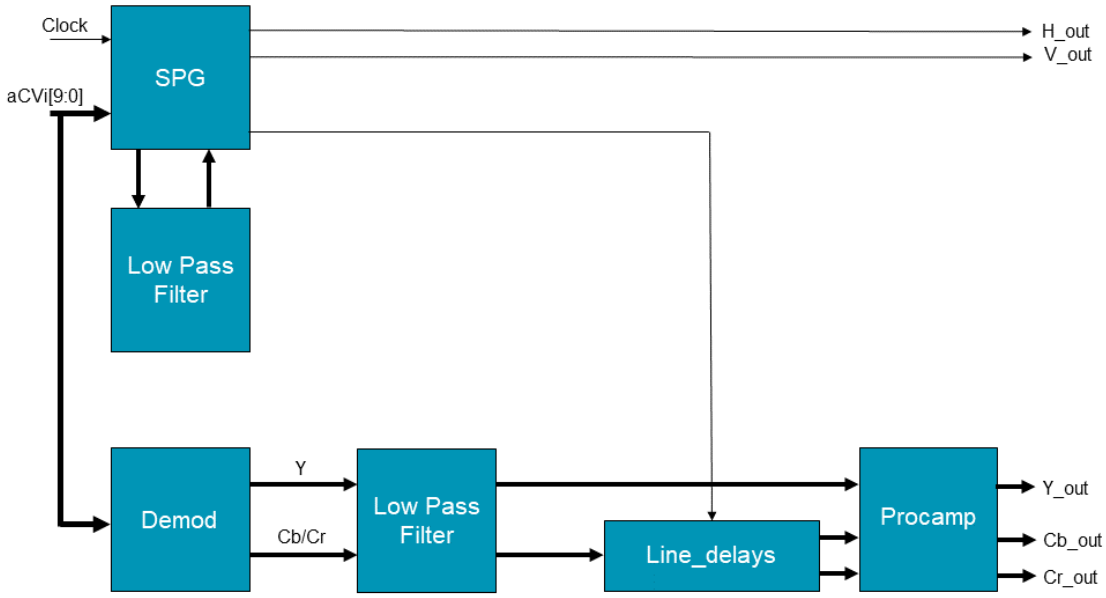

Figure 25 aCVi decoder block diagram.

The aCVi input is the output from the sample rate converter and is converted to 10-bit 2'complement video sampled at 74.25MHz/74.18MHz.

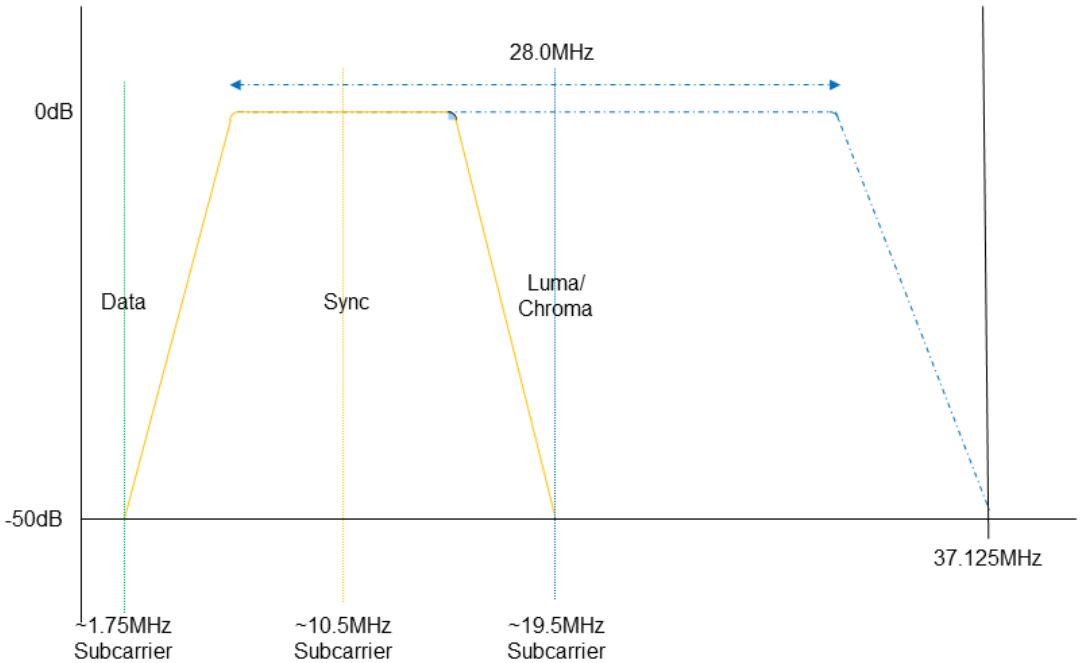

Figure 26 aCVi spectrum.

aCVi_SPG.v

The digital aCVi video is received by the SPG.v (Sync Pulse Generator) module. A ratio counter generates the sync subcarrier frequency as shown in Table 4 (approximately 10.5MHz). The top 11 bits of the ratio counter (phase value) address sine and cosine lookup tables. The sine and cosine waveforms are multiplied by the aCVi video input.

Standard	Pixels/line	Line frequency	Clock frequency	Horizontal sync width (clocks)	Broad pulse start position (clocks)	Broad pulse end position (clocks)	Burst gate start position (clock periods)	Video Subcarrier frequency	Sync Subcarrier frequency
720p/23Hz	4125	17.982kHz	74.18MHz	80	296	3755	151	19.465534MHz	10.471528MHz
720p/24Hz	4125	18.000kHz	74.25MHz	80	296	3755	151	19.503MHz	10.500000MHz
720p/25Hz	3960	18.750kHz	74.25MHz	80	296	3590	151	19.509375MHz	10.50625MHz
720p/29Hz	3300	22.477kHz	74.18MHz	80	296	2930	151	19.454296MHz	10.482018MHz
720p/30Hz	3300	22.500kHz	74.25MHz	80	296	2930	151	19.49625MHz	10.500000MHz
720p/50Hz	1980	37.500kHz	74.25MHz	80	296	1610	151	19.51875MHz	10.5125MHz
720p/59Hz	1650	44.955kHz	74.18MHz	80	296	1280	151	19.420579MHz	10.489510MHz
720p/60Hz	1650	45.000kHz	74.25MHz	80	296	1280	151	19.5075MHz	10.500000MHz
1080p/23Hz	2750	26.973kHz	74.18MHz	80	236	1920	121	19.461039MHz	10.474525MHz
1080p/24Hz	2750	27.000kHz	74.25MHz	80	236	1920	121	19.5075MHz	10.485000MHz
1080p/25Hz	2640	28.125kHz	74.25MHz	80	236	1920	121	19.5046875MHz	10.500000MHz
1080p/29Hz	2200	33.716kHz	74.18MHz	80	236	1920	121	19.471154MHz	10.463287MHz
1080p/30Hz	2200	33.750kHz	74.25MHz	80	236	1920	121	19.490625MHz	10.5075MHz

Table 6 PT54 aCVi standards.

The output of the multipliers is low pass filtered using a 23-tap FIR filter. The response of this filter is shown in Figure 27.

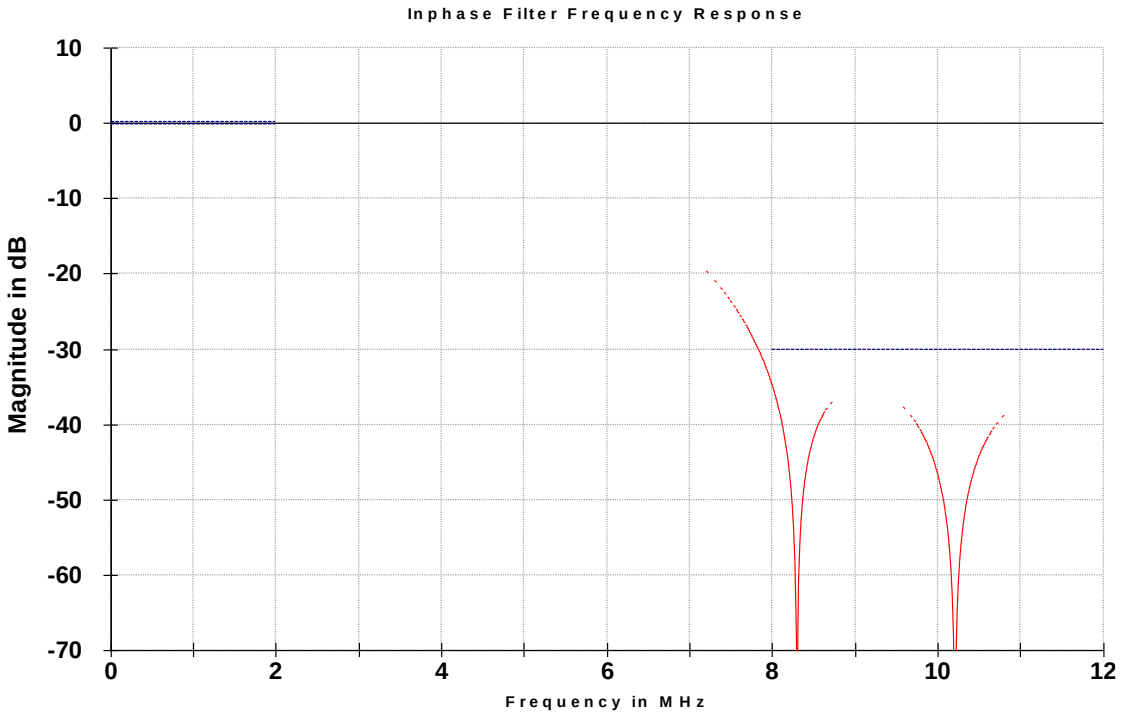

Figure 27 Frequency characteristic of the aCVi Sync demodulation low pass filter.

The low pass filtered sine channel is used as the frequency/phase reference to lock the demodulator and the cosine channel is the demodulated sync waveform. The sync pulse generator provides a gating pulse which occurs during the modulated sync burst. 32 samples of the low pass filtered sine waveform are accumulated each horizontal line. When the free-running output of the ratio counter and the frequency and phase of the aCVi input sync are aligned this accumulated value will be zero. Otherwise it adjusts the phase and frequency of the ratio counter until they are.

When the sync demodulator loop is locked, we will have correctly demodulated the sync waveform. The recovered horizontal sync waveform is shown in Figure 28.

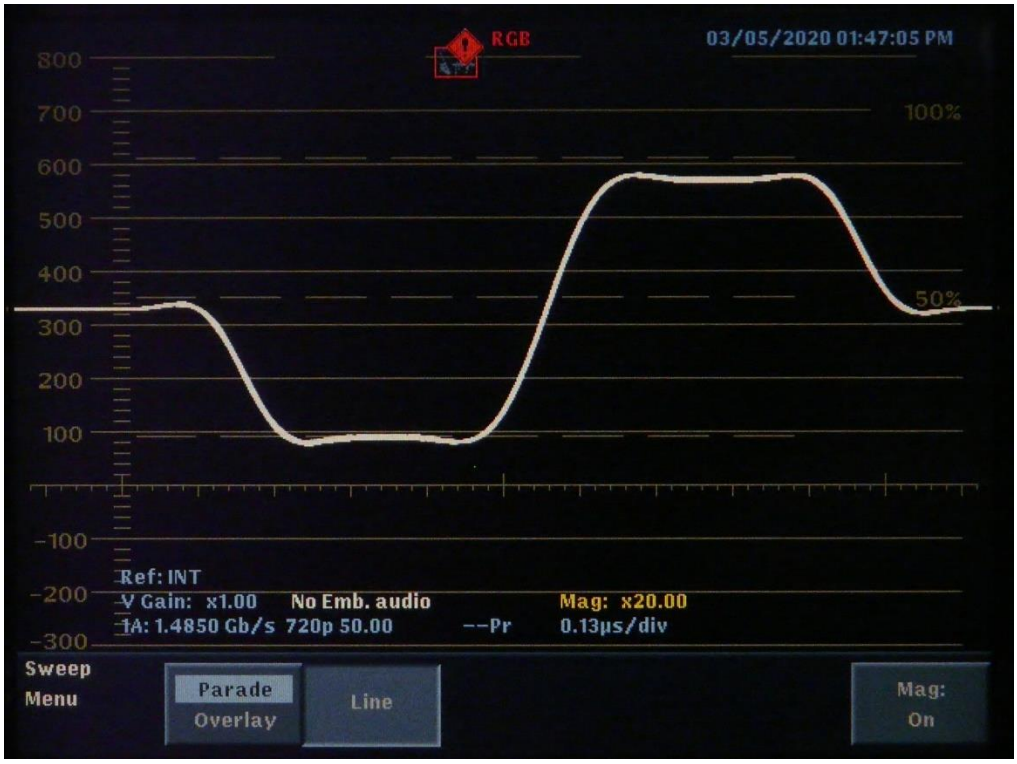

Figure 28 Demodulated horizontal sync waveform.

A free-running counter generates a horizontal sync pulse for the appropriate video standard. 32 of these counts address a lookup table which supplies coefficients to a FIR filter. This filter further reduces noise and its response is shown in Figure 29. The coefficients are multiplied by the low pass filtered cosine channel and accumulated. If the 32 samples align with the sync waveform their accumulated value will be zero. Otherwise the accumulated value is filtered and used to control a pulse width modulated output (VCO_PWM) which in turn adjust the frequency of a voltage-controlled oscillator (see Chapter 6). The frequency of the VCO is therefore adjusted until the free-running and the recovered sync waveforms align.

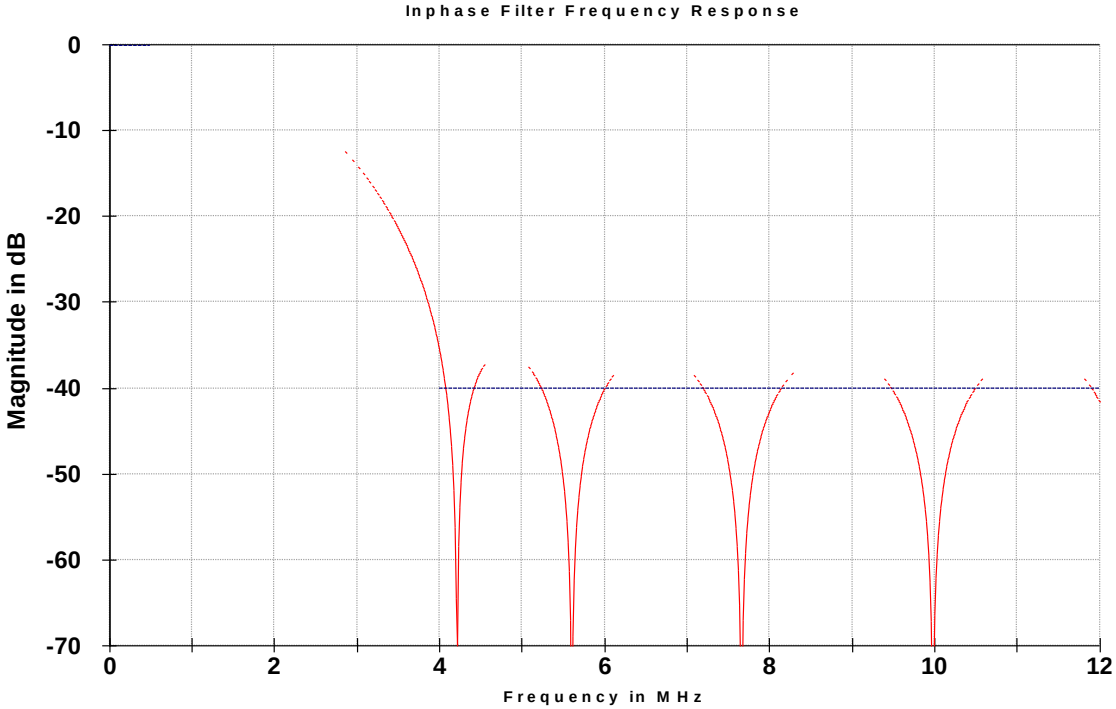

Figure 29 Frequency characteristic of the Sync phase detector.

The vertical sync recovery detects the wide broad pulses (see Figure 30) during the vertical interval by integrating the low pass filtered cosine values and thresholding the integrated values. The narrow horizontal pulses do not pass the threshold, but the wide broad vertical pulses do.

The SPG modules then regenerates the horizontal and vertical timing signals required by the PT54 decoder. The H_out and V_out sync pulses may be moved relative to the video to match and subsequent module's timing requirements.

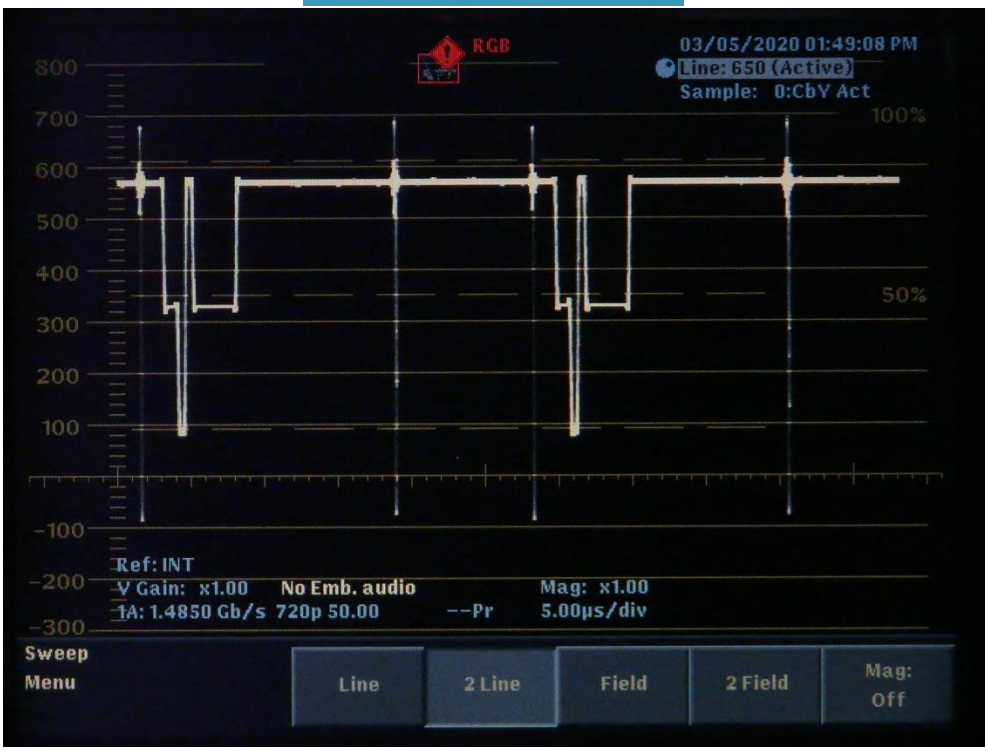

Figure 30 Demodulated Vertical sync waveform.

aCVi_Demod.v

Another ratio counter generates the video subcarrier value as shown in Table 6. Sine and Cosine waveforms are generated at this frequency which are then multiplied by the digital aCVi video and low pass filtered. The low pass filter is a 47-tap FIR with a response as shown in Figure 31.

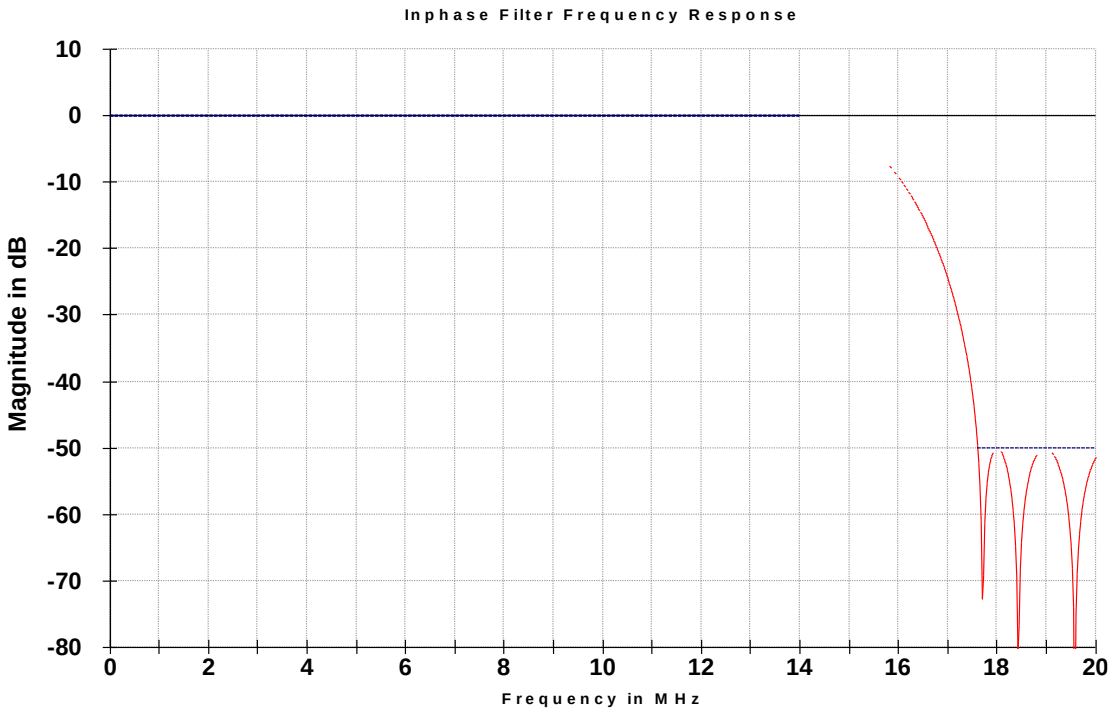

Figure 31 Frequency characteristic of the aCVi video demodulation low pass filter.

The sine channel is the demodulated luma (Y) video and the cosine channel is the line-multiplexed chroma (Cb and Cr) video. A SPG module produces a gate pulse which samples the burst sample of the video subcarrier and from it generates an error signal which modifies the video demodulation ratio counter to achieve phase and frequency lock of the video demodulation loop.

Line_delays.v

aCVi_Proc_amp.v

The SPG module generates a half horizontal frequency signal. The multiplexed Cb/Cr chroma is the data input to two line stores. For each horizontal one of the line stores is writing and one is reading. For example, if the chroma for the video line is Cb video, this is routed directly through to the Cb output whilst also being written into one of the line stores. On the next line (Cr video) the Cb output is read from the previously written line store. The sequence is the opposite for the Cr output.

The Proc-amp.v (Processing amplifier) module condition the video for the PT54 output. The module applies gain, clipping and blanking to the output signal so that it conforms with the BT1120 output specification. The video outputs are valid on the rising edge of the Clock signal. The YCbCr aCVi output are multiplexed with the YCbCr output from the NTSC/PAL/AHD Procamp depending on the video format.

8. Register interface

Figure 32 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via a 7-bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT54_CSn (chip select) input must be asserted low and the A[6:0] register address and the data for this register set up. The PT54_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT54_CSn input should then be returned high.

For the write to occur reliably the address (A[6:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT54_WRn pulse.

The address input also selects the register data that is presented on the Register_out[7:0] bus. This output is independent of the PT54_CSn or PT54_WRn inputs.

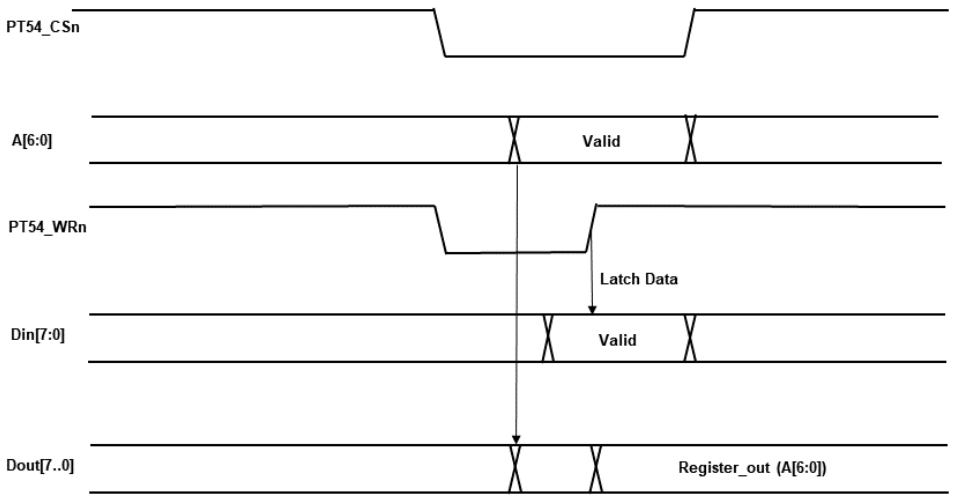

Figure 32 PT54 Register timing.

9. Register descriptions

Table 8 lists all of the control and status registers. All of the registers are 8-bit; unused register bits read back as zeros.

Please note that some registers can be set to values that are illegal and will produce invalid outputs.

Asserting the RESETn input resets the PT54 registers to their default values.

Register Offset	Register Name	R/W	Bit Value	Description	
Control Registers					
$00	**Control_1**	R/W			
	Auto standard		7	If reset to '0' the video standard is preset manually using bits 6:0. If set to '1' (default value) the detected video standard is determined automatically.	
	Video standard		6:0	Video standard [6:0] (decimal)	Standard
				0	NTSC-M
				1	PAL
				16	720p/23 (aCVi only)
				17	720p/24 (aCVi only)
				18	720p/25
				19	720p/29 (aCVi only)
				20	720p/30
				21	720p/50 (aCVi only)
				22	720p/59 (aCVi only)
				23	720p/60 (aCVi only)
				24	1080p/23 (aCVi only)
				25	1080p/24 (aCVi only)
				26	1080p/25
				27	1080p/29 (aCVi only)
				28	1080p/30
				35	960p/30 (AHD only)
				96	1440p/25Hz (4MP) (AHD only)
				97	1440p/30Hz (4MP) (AHD only)
				98	1980p/12.5Hz (5MP) (AHD only)
				99	1980p/20Hz (5MP) (AHD only)
$01	**Control_2**	R/W			
	Auto register		7	If set to '1' (default value) the parameter values are set to their default values depending on the video standard (note: only those standards listed in bits [3:0] have default values assigned). If set to '0', Registers $20-$4F may be programmed manually.	
			6:3	Not used	
	Auto comb mode		2	In SD mode only (Control 1 bits 6:4 = '000'), if set to '1', the comb mode is set automatically depending on the comb failure detection logic. If set to '0' the comb mode is manually set using the manual comb mode bits [3:0].	
			1	Not used	
	Manual comb mode		0	Bit 0	If the auto comb mode is set to '0'.
				0	Forces low pass mode.
				1	Forces line comb mode
$02	**Control_3**	R/W	7	Not used.	
			6	Bypasses the sample rate converter if set to '1'. If set to '0' the sample rate converter operates, and the input clock should be a fixed frequency.	
			5:4	Bits [5:4]	VCO_PWM output
				00	Error output (VCO lock mode)
				01	Force VCO_PWM output to '0'.
				10	Force VCO_PWM output to '1'.
				11	Force VCO_PWM output to 50% (SRC mode when using a VCO for

Register Offset	Register Name	R/W	Bit Value	Description
				the clock).
			3:1	Not used.
	ABL		0	Enables the automatic black level if set to '1'. The back porch value is measured and subtracted from the composite video (effectively removing the sync pulses from the luma output). If ABL is turned off, a fixed DC offset set by registers $30 and $31 is subtracted from the output.
				Procamp
$08	**Sub_Luma_value_1**	R/W	7:0	Value subtracted from luma output (to remove synchronizing pulses), if ABL = 0 (Control3[0]). 10 bit word = ({Sub_Luma_value_2[1:0],Sub_Luma_value_1[7:0]}). Default value = 150_{10}.
$09	**Sub_Luma_value_2**	R/W	1:0	
$0A	**Ygain_value_1**	R/W	7:0	Luma gain control. 10 bit word = ({Ygain_value_2[1:0],Ygain_value_1[7:0]}). Default value = 746_{10}.
$0B	**Ygain_value_2**	R/W	1:0	
$0C	**Ugain_value_1**	R/W	7:0	Chroma (B-Y) gain control. 10 bit word = ({Ugain_value_2[1:0],Ugain_value_1[7:0]}). Default value = 512_{10}.
$0D	**Ugain_value_2**	R/W	1:0	
$0E	**Vgain_value_1**	R/W	7:0	Chroma (R-Y) gain control. 10 bit word = ({Ugain_value_2[1:0],Ugain_value_1[7:0]}). Default value = 512_{10}.
$0F	**Vgain_value_2**	R/W	1:0	
				SPG
$20	**Hcount_length_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hcount Length is preset according to the selected standard. If set to '0', Hcount Length can be programmed manually using these 2 registers: ({Hcount Length_2[3:0], Hcount Length_1[7:0]}). The value is the total number of pixels per line - 1.
$21	**Hcount_length_2**	R/W	3:0	
$22	**Hout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hout_start is preset according to the selected standard. If set to '0', Hout_start can be programmed manually using these 2 registers: ({Hout_start_2[3:0], Hout_start_1[7:0]}). The value is the position of the falling edge of the Hout sync pulse w.r.t. to the falling edge of the input horizontal sync pulse.
$23	**Hout_start_2**	R/W	3:0	
$24	**Hout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Hout_end is preset according to the selected standard. If set to '0', Hout_end can be programmed manually using these 2 registers: ({Hout_end_2[3:0], Hout_end_1[7:0]}). The value is the position of the rising edge of the Hout sync pulse w.r.t. to the falling edge of the input horizontal sync pulse.
$25	**Hout_end_2**	R/W	3:0	
$26	**HBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' HBlank_start is preset according to the selected standard. If set to '0', HBlank_start can be programmed manually using these 2 registers: ({HBlank_start_2[3:0], HBlank_start_1[7:0]}). The value is the position of the beginning of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$27	**HBlank_start_2**	R/W	3:0	
$28	**HBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' HBlank_end is preset according to the selected standard. If set to '0', HBlank_end can be programmed manually using these 2 registers: ({HBlank_end_2[3:0], HBlank_end_1[7:0]}). The value is the position of the end of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$29	**HBlank_end_2**	R/W	3:0	
$2A	**Halfline_set_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Halfline_set is preset according to the selected standard. If set to '0', Halfline_set can be programmed manually using these 2 registers: ({Halfline_set_2[3:0], Halfline_set_1[7:0]}). The value is the position of the beginning of blanking w.r.t. to the falling edge of the input horizontal sync pulse.
$2B	**Halfline_set_2**	R/W	3:0	
$2C	**Burst_gate_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate start is preset according to the selected standard. If set to '0', Burst gate start can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse for the beginning of the burst gate.
$2D	**Burst_gate_start_2**	R/W	3:0	
$2E	**Burst_gate_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate end is preset according to the selected standard. If set to '0', Burst gate end can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse until the end of the burst gate.
$2F	**Burst_gate_end_2**	R/W	3:0	
$2C	**Back_porch_start_**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate start is preset

Register Offset	Register Name	R/W	Bit Value	Description
	1			according to the selected standard. If set to '0', Burst gate start can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse for the beginning of the burst gate.
$2D	**Back_porch_start_ 2**	R/W	3:0	
$2E	**Burst_gate_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' Burst gate end is preset according to the selected standard. If set to '0', Burst gate end can be programmed manually using these 2 registers: ({Burst_gate_start _2[3:0], Burst_gate_start _1[7:0]}). The value is the number of clocks after the falling edge of the input horizontal sync pulse until the end of the burst gate.
$2F	**Burst_gate_end_2**	R/W	3:0	
$30	**Vout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout_start is preset according to the selected standard. If set to '0', Vout start can be programmed manually using these 2 registers: ({Vout_start_2[2:0], Vout_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Vout output.
$31	**Vout_start_2**	R/W	2:0	
$32	**Vout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout_end is preset according to the selected standard. If set to '0', Vout end can be programmed manually using these 2 registers: ({Vout_end_2[2:0], Vout_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Vout output.
$33	**Vout_end_2**	R/W	2:0	
$34	**Vout2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout2_start is preset according to the selected standard. If set to '0', Vout2 start can be programmed manually using these 2 registers: ({Vout2_start_2[2:0], Vout2_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Vout output for the interlaced field. For non-interlaced formats this register should be set to the same value as Vout_start.
$35	**Vout2_start_2**	R/W	2:0	
$36	**Vout2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Vout2_end is preset according to the selected standard. If set to '0', Vout2 end can be programmed manually using these 2 registers: ({Vout2_end_2[2:0], Vout2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Vout output for the interlaced field. For non-interlaced formats this register should be set to the same value as Vout_end.
$37	**Vout2_end_2**	R/W	2:0	
$38	**Fout_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Fout_start is preset according to the selected standard. If set to '0', Fout start can be programmed manually using these 2 registers: ({Fout_start_2[2:0], Fout_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the falling edge of the Fout output. This register is only valid for interlaced video formats.
$39	**Fout_start_2**	R/W	2:0	
$3A	**Fout_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the Fout_end is preset according to the selected standard. If set to '0', Fout end can be programmed manually using these 2 registers: ({Fout_end_2[2:0], Fout_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the rising edge of the Fout output. This register is only valid for interlaced video formats.
$3B	**Fout_end_2**	R/W	2:0	
$3C	**VBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank_start is preset according to the selected standard. If set to '0', VBlank start can be programmed manually using these 2 registers: ({VBlank_start_2[2:0], VBlank_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of vertical blanking.
$3D	**VBlank_start_2**	R/W	2:0	
$3E	**VBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank_end is preset according to the selected standard. If set to '0', VBlank_end can be programmed manually using these 2 registers: ({VBlank_end_2[3:0], VBlank_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of vertical blanking.
$3F	**VBlank_end_2**	R/W	2:0	
$40	**VBlank2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank2_start is preset

Register Offset	Register Name	R/W	Bit Value	Description
$41	**VBlank2_start_2**	R/W	2:0	according to the selected standard. If set to '0', VBlank2 start can be programmed manually using these 2 registers: ({VBlank2_start_2[2:0], VBlank2_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$42	**VBlank2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the VBlank2_end is preset according to the selected standard. If set to '0', VBlank2 end can be programmed manually using these 2 registers: ({VBlank2_end_2[2:0], VBlank2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$43	**VBlank2_end_2**	R/W	2:0	
$44	**SVBlank_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank_start is preset according to the selected standard. If set to '0', SVBlank start can be programmed manually using these 2 registers: ({SVBlank_start_2[2:0], SVBlank_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of short vertical blanking.
$45	**SVBlank_start_2**	R/W	2:0	
$46	**SVBlank_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank_end is preset according to the selected standard. If set to '0', SVBlank_end can be programmed manually using these 2 registers: ({SVBlank_end_2[3:0], SVBlank_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of short vertical blanking.
$47	**SVBlank_end_2**	R/W	2:0	
$48	**SVBlank2_start_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank2_start is preset according to the selected standard. If set to '0', SVBlank2 start can be programmed manually using these 2 registers: ({SVBlank2_start_2[2:0], SVBlank2_start_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the beginning of short vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$49	**SVBlank2_start_2**	R/W	2:0	
$4A	**SVBlank2_end_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the SVBlank2_end is preset according to the selected standard. If set to '0', SVBlank2 end can be programmed manually using these 2 registers: ({SVBlank2_end_2[2:0], SVBlank2_end_1[7:0]}). The value is the number of horizontal lines after the falling edge of the vertical sync (field or frame if interlaced input) for the end of short vertical blanking for the interlaced field. This register is only valid for interlaced video formats.
$4B	**SVBlank2_end_2**	R/W	2:0	
$4C	**FSc_1**	R/W	7:0	If Control register 1, bit 7 is set to '1' the subcarrier frequency seed is preset according to the selected standard. If set to '0', the subcarrier frequency seed can be programmed manually using these 4 registers: ({FSc_1[7:0], FSc_2[7:0], FSc_3[7:0], FSc_4[7:0]}). The seed is a 32 bit number and FSc_1[7] is the MSB. Default value is 55693156_H
$4D	**FSc_2**	R/W	7:0	
$4E	**FSc_3**	R/W	7:0	
$4F	**FSc_4**	R/W	7:0	
Status				
$6D	**Status**	R	7:1	Not used
			0	Horizontal lock detect.

Table 7 Register description.