singmai

PT55

Advanced Composite Video Interface: Encoder IP Core

User Manual

Revision 1.1
16th November 2018

Revisions

Date	Revisions	Version
01-05-2016	First Draft.	0.1
28-05-2106	Timing diagrams updated. Block diagram updated.	0.2
13-07-2016	1080i standards added. IP core resource usage added. aCVi description modified. Data transfer description added. Cable compensation description added. Simulation information added. Altera encryption description added.	0.3
17-07-2016	FPGA resource use updated. Reg_clk port removed. Insertion test signal modified. Data transmit register locations corrected. Register address range changed to A[4:0]. Text corrections and additions.	0.4
09-08-2016	Luma interpolation added. Chroma interpolation filter modified. Subcarrier frequencies modified. aCVi description modified. Data slicing schematic updated. Output interface schematic updated.	0.5
25-08-2016	Verilog modules renamed. Some ports renamed. NTSC-M/PAL/NTSC-960H and PAL-960H standards added. SD chroma filters added. Input formatting added.	0.6
21-09-2016	aCVi 0.5 format added.	0.7
11-11-2016	aCVI 0.5 format removed. Changes to data transfer control. Changes to auto cable compensation. Additional luma interpolation filter added (for alternative analogue HD formats). Chroma interpolation filter redesigned.	0.8
06-09-2018	960H select bit reassigned (Control 1). SD/HD select b it reassigned (Control 1). NTSC/PAL standard select bits reassigned (Control 1). Video format register bits added (Control 1). Removed the input format control (30 bit YCbCr input only – Control 2). Y interpolation filter reduced in size. Cb/Cr interpolation filter reduced in size.	0.9
06-10-2018	Document reformatted. Added register controls for SPG. Added 1280H support. Removed data module. Register address input increased by 2 bits (A[6:0]) Reduced size of luma interpolator filter. Added more chroma interpolator filters.	1.0

Date	Revisions	Version
	Top level interconnections changed. 4:4:4 mode removed.	
16-10-2018	Luma filter extended to 47 taps to include HD-CVI and HD-TVI support. HD-TVI chroma filter added. HD format table added.	1.1

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1. Introduction

PT55 is an aCVi encoder IP (intellectual property) core compatible with the aCVi Advanced Composite Video Interface. aCVi is a method to transmit high quality HD video over long distances of coaxial or twisted-pair cable.

The encoder IP accepts YCbCr digital component data with either embedded or separate syncs which it encodes to a single 10 bit straight binary composite output for driving a suitable DAC (digital to analogue converter) and amplifier. PT55 supports 720p-25Hz/30Hz/50Hz/60Hz and 1080p-25Hz/30Hz input HD video formats which it encodes to aCVi as well as other HD analogue formats.

In addition, the PT55 will also encode 525i and 625i formatted data to NTSC-M/NTSC-960H/NTSC-1280H or PAL/PAL-960H/PAL-1280H formats respectively.

Control and status registers are written to and read from using a conventional 8-bit wide microprocessor interface.

The intellectual property block is provided as RTL compliant Verilog-2001 source code for FPGAs from all vendors or for ASICs.

Typical resource usage for an Altera FPGA (compiled for a Cyclone IV EP4CE15 device) is shown in Table 1.

Logic Cells	Memory Bits	M9K blocks	9x9 Multipliers	18x18 multipliers
7913	12288	2	0	56
15362	12288	2	0	0

Table 1 PT55 Altera FPGA resource requirements

An approximate equivalent for ASIC resource usage is 15362 LCs (logic cell only compile for Altera FPGA) x 14 ~ 215k 2 input NAND gate equivalent. The memory is 13kb of single port ROM (512 x 24).

2. Module Description

The PT55 aCVi encoder IP core comprises 8 Verilog modules in a hierarchical structure, (see Table 2).

aCVi_encoder.v	aCVI_Register_control.v	
	aCVi_Cin.v	
	aCVi_Yin.v	
	aCVI_Tx_SPG.v	
	aCVi_Modulator.v	Tx_SinCos_ROM.v
	aCVi_Preemphasis.v	

Table 2 PT55 Verilog file structure.

The top level file is aCVi_encoder.v which, in turn, calls six of the other modules. aCVi_Modulator.v calls a third level file, Tx_SinCos_ROM.v.

3. Signal Interconnections

The PT55 signal interconnect diagram is shown in Figure 1.

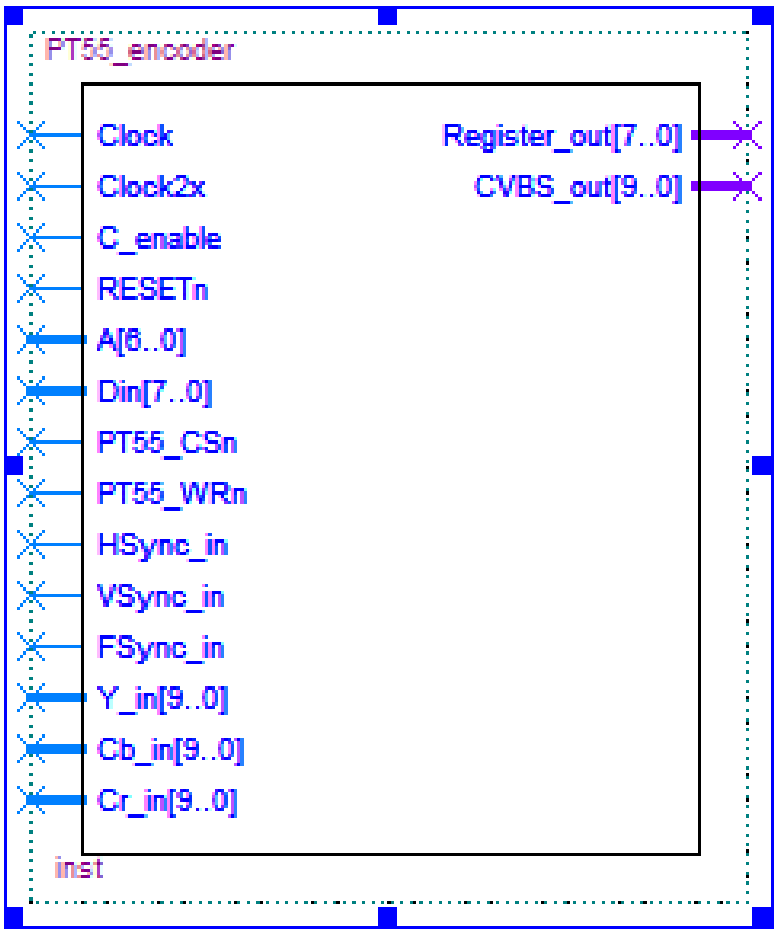

Figure 1 PT55 Block schematic.

The signal descriptions are shown in Table 3, below.

Inputs	
Signal	**Description**
Clock	Input clock (74.25MHz for HD[1], 13.5MHz for NTSC-M/PAL, 18MHz for NTSC-960H/PAL-960H and 22.5MHz for NTSC-1280H/PAL-1280H). All data inputs should be valid at the rising edge of this clock.
Clock2x	Twice the Clock input frequency (148.5MHz[2], 27MHz/36MHz/45MHz for NTSC/PAL). Output data is valid on the rising edge of this clock. The rising edges of Clock and Clock2x should be coincident.
C_enable	Used for demultiplexing the 4:2:2 20 bit input. (See p.12.)
RESETn	Asynchronous active low reset signal. Asserting this input sets all the control registers to their default value and resets all registers.
A[6:0]	Control address bus input used to select the control register to be written to/read from.
Din[7:0]	Control data input bus.
PT55_CSn	Control chip select input, active low. Used in combination

	with the WRn input to control writing to the control registers. (See Chapter 6.)
PT55_WRn	Active low write enable input. Used in combination with the CSn input to control writing to the control registers. (See Chapter 6.)
HSync_in	Horizontal synchronization input. For 720p/60Hz operation this input is at 45kHz. Active low input, the falling edge is the 0H timing reference point. This input must be at least 4 'Clock' periods wide. (See p.12.)
VSync_in	Vertical synchronization input. For 720p/60Hz operation this input is at 60Hz. Active low input, the falling edge is the 0V timing reference point. This input must be at least 4 'Clock' periods wide. (See p.12.)
FSync_in	Frame synchronization input. For interlaced inputs this input indicates the first (='0') or second ('1') field of the frame. For non-interlaced inputs this input should be tied to '0'. (See Table 6.)
Y_in[9:0]	Y (luma) input or BT1120 Y component input to the encoder. If luma, the input is straight binary, blanking level is 64_{10} and peak level 960_{10}. The data input should be valid at the rising edge of 'Clock'. Y_in[9] is the MSB. If the input is 8-bits wide, the bottom 2 bits should be tied to '0'. (See Table 6.)
Cb_in[9:0]	Cb (B-Y chroma) input or Cb/Cr multiplexed input to the encoder or BT1120 chroma component. The input is offset binary, blanking level is 512_{10}. The data input should be valid at the rising edge of 'Clock'. Cb_in[9] is the MSB. If the input is 8-bits wide, the bottom 2 bits should be tied to '0'. (See Table 6.)
Cr_in[9:0]	Cr (R-Y chroma) input to the encoder. The input is offset binary, blanking level is 512_{10}. The data input should be valid at the rising edge of 'Clock'. Cr_in[9] is the MSB. If the input is 8-bits wide, the bottom 2 bits should be tied to '0'. (See Table 6).
Outputs	
Signal	**Description**
Register_out[7:0]	Control output data bus. Outputs the control/status register data selected by the A[6:0] bus.
CVBS_out[9:0]	Encoded composite video output data. CVBS_out[9] is the MSB. The output is straight binary coded and is valid at the rising edge of 'Clock2x'.

[1] The Clock frequency for AHD 720p/25Hz and 720p/30Hz is 72MHz.
[2] The Clock2x frequency for AHD 720p/25Hz and 720p/30Hz is 144MHz.

Table 3 PT55 Input/Output signals

The Verilog instantiation of PT55 is shown below:

```
PT55_encoder PT55_encoder_inst
(
.Clock(Clock_sig) ,                    // input  Clock_sig
.Clock2x(Clock2x_sig) ,                // input  Clock2x_sig
.C_enable(C_enable_sig) ,              // input  C_enable_sig
.RESETn(RESETn_sig) ,                  // input  RESETn_sig
.A(A_sig) ,                            // input [6:0] A_sig
.Din(Din_sig) ,                        // input [7:0] Din_sig
.PT55_CSn(PT55_CSn_sig) ,              // input  PT55_CSn_sig
.PT55_WRn(PT55_WRn_sig) ,              // input  PT55_WRn_sig
.HSync_in(HSync_in_sig) ,              // input  HSync_in_sig
.VSync_in(VSync_in_sig) ,              // input  VSync_in_sig
.FSync_in(FSync_in_sig) ,              // input  FSync_in_sig
.Y_in(Y_in_sig) ,                      // input [9:0] Y_in_sig
.Cb_in(Cb_in_sig) ,                    // input [9:0] Cb_in_sig
.Cr_in(Cr_in_sig) ,                    // input [9:0] Cr_in_sig

.Register_out(Register_out_sig) ,      // output [7:0] Register_out_sig
.CVBS_out(CVBS_out_sig)                // output [9:0] CVBS_out_sig
);
```

4. aCVi Overview

TBD.

Format	Pixels/line	Line frequency	F_{SC}/F_H ratio	Subcarrier
720p/25Hz	3960	18.75kHz		
720p/30Hz	3300	22.5kHz		
720p/50Hz	1980	37.500kHz		
720p/60Hz	1650	45.000kHz		
1080p/24Hz	2750	27.0kHz		
1080p/25Hz	2640	28.125kHz		
1080p/30Hz	2200	33.750kHz		

Table 4 aCVi supported video formats.

5. Technical Overview

A simplified block diagram of the PT55 encoder is shown in Figure 2.

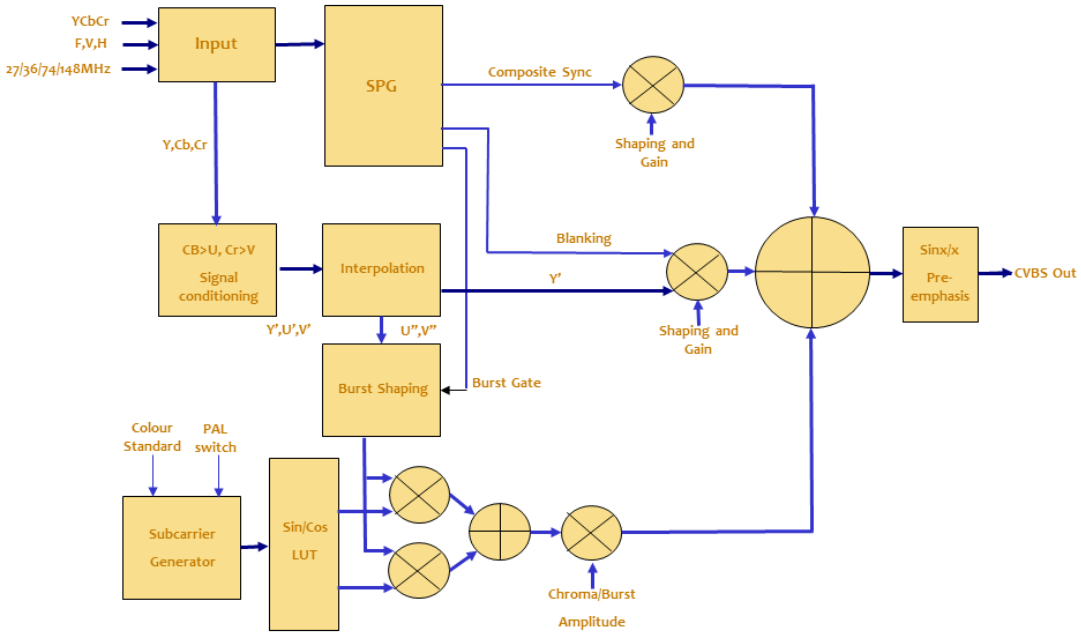

Figure 2 PT55 Block diagram.

PT55_encoder.v

This is the top level design file and it interconnects all the following modules.

Table 5 shows the input parameters for the default supported formats and Table 6 the measured parameters for the HD formats.

Format	Pixels/line	Line frequency	Clock/Clock2x frequency	Subcarrier frequency	Sync Ampl.	Burst Ampl.	Luma Video	75% Bars Yellow Chroma
720p/25Hz AHD	1920	18.75kHz	36.0/72.0MHz	11.466MHz	300mV	225mV	700mV	
720p/30Hz AHD	1600	22.5kHz	36.0/72.0MHz	11.44MHz	300mV	225mV	700mV	
1080p/25Hz AHD	2640	28.125kHz	74.25/148.5MHz	23.92MHz	300mV	225mV	700mV	
1080p/30Hz AHD	2200	33.750kHz	74.25/148.5MHz	24.015861MHz	300mV	225mV	700mV	
NTSC-M	858	15.734kHz	13.5/27.0MHz	3.5795455MHz	286mV	286mV	714mV	443mV
PAL	864	15.625kHz	13.5/27.0MHz	4.43361875MHz	300mV	300mV	700mV	470mV
NTSC-960H	1144	15.734kHz	18.0/36.0MHz	3.5795455MHz	286mV	286mV	714mV	443mV
PAL-960H	1152	15.625kHz	18.0/36.0MHz	4.43361875MHz	300mV	300mV	700mV	470mV
NTSC-1280H	1430	15.734kHz	22.5/45.0MHz	3.5795455MHz	286mV	286mV	714mV	443mV
PAL-1280H	1440	15.625kHz	22.5/45.0MHz	4.43361875MHz	300mV	300mV	700mV	470mV

Table 5 Input format parameters.

Format		Active Width	Active Height	Line active area	Color subcarrier	Horizontal sync width	Start of burst	Start of line active area
TVI	720p25	1280	720	17.15µs	42.1MHz	1.065µs	1.33µs	3.955µs
	720p30			17.1µs	42.19MHz	1.065µs	1.30µs	3.945µs
	720p50			17.1µs	42.02MHz	1.07µs	1.32µs	4.04µs
	720p60			17.15µs	42.35MHz	1.07µs	1.305µs	3.985µs
	1080p25	1920	1080	25.75µs	42MHz	1.19µs	1.35µs	3.19µs
	1080p30			25.7µs	43.02MHz	1.185µs	1.35µs	3.18µs
CVI	720p25	1280	720					
	720p25			42.6µs	21.05MHz	3.89µs	4.71µs	9.33µs
	720p30							
	720p30			35.5µs	21.0MHz	3.24µs	3.92µs	7.76µs
	720p50							
	720p60							
	1080p25	1920	1080	28.4µs	38.02MHz	2.61µs	3.05µs	6.2µs
	1080p30			23.68µs	37.88MHz	2.18µs	2.531µs	5.175µs
AHD	720p25	1280	720	35.35µs	11.4MHz	3.325µs	4.26µs	7.49µs
	720p30			35.0µs	11.435MHz	3.335µs	4.25µs	7.47µs
	720p50			35.45µs	11.39MHz	3.32µs	4.19µs	7.42µs
	720p60			35.45µs	11.425MHz	3.32µs	4.22µs	7.44µs
	1080p25	1920	1080	25.8µs	23.92Mhz	2.01µs	2.35µs	3.43µs
	1080p30			25.8µs	23.98MHz	2.03µs	2.35µs	3.41µs

Table 6 Measured HD formats timing.

Register_control.v

A conventional 8 bit microprocessor style control interface is used to write and read to the PT55 control registers. Details of the interface may be found in Chapter 6 and the register descriptions may be found in Chapter 7.

Yin.v

The PT55 can accept 3 different formats of video input as described in Table 7. Selection of the input format is made using Control register 2, bits [2:0].

Input format	Y_in[9:0]	Cb_in[9:0]	Cr_in[9:0]	Comments
4:2:2	Y input	Cb input	Cr input	Separate Y/Cb/Cr inputs (30 bits, 4:2:2 mode). Y is clocked with 'Clock'; Cb/Cr are clocked with if 'C_enable' is '1'. Synchronising inputs are HSync_in, VSync_in and FSync_in (if interlaced).
4:2:2	Y input	Cb/Cr input	Not used	Separate Y and multiplexed Cb/Cr inputs (20 bits). Y is clocked with 'Clock'; Cb/Cr are clocked with 'Clock' with either 'C_enable' signaling which is Cb (= '0') or Cr (= '1') or the demultiplexing signal being derived from the HSync_in input. Synchronising inputs are HSync_in, VSync_in and FSync_in (if interlaced).
4:2:2	BT1120 input [19:10]	BT1120 input [9:0] (Cb/Cr[9:0])	Not used	Multiplexed Y/Cb/Cr inputs (20 bits). BT1120 input is clocked with 'Clock'. Synchronising inputs are extracted from the BT1120 input (TRS).

Input format	Y_in[9:0]	Cb_in[9:0]	Cr_in[9:0]	Comments
	(Y[9:0])			

Table 7 PT55 Input video formats.

The two methods of demultiplexing the chroma in 20 bit mode are illustrated in Figure 3.

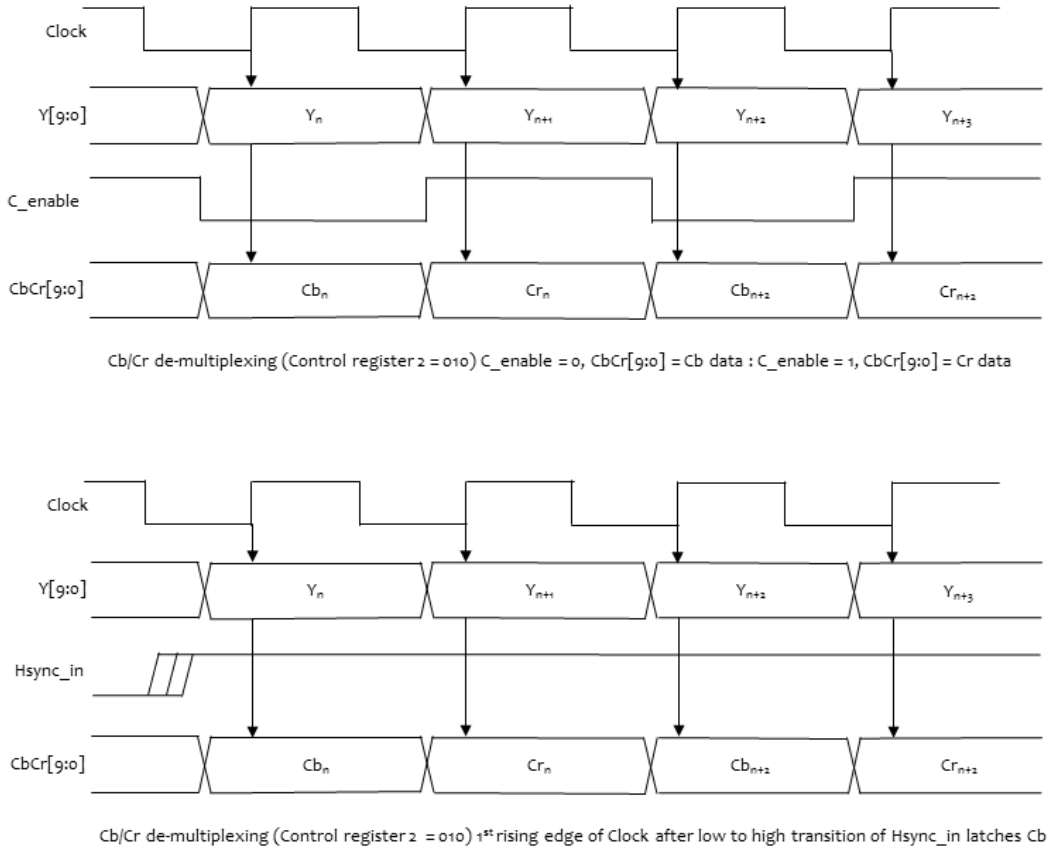

Figure 3 Input chroma demultiplexing modes.

The luma signal is interpolated from 'Clock' frequency to 'Clock2x' frequency using a 47 tap FIR filter: e.g. for NTSC/PAL the 13.5MHz Y input is interpolated to 27MHz. The appropriate filter is selected automatically based on the standard selected by Control Register 1.

For NTSC-M and PAL (27MHz output) the passband is 5.25MHz and the stop band of 6.75MHz. The NTSC/PAL bandwidth was reduced to save on the filter size and is allowable as the NTSC/PAL output is only used for monitoring purposes. For 960H and 1280H operation (36/45MHz outputs) the same filter is used giving proportionally higher luma bandwidths (see Figure 4).

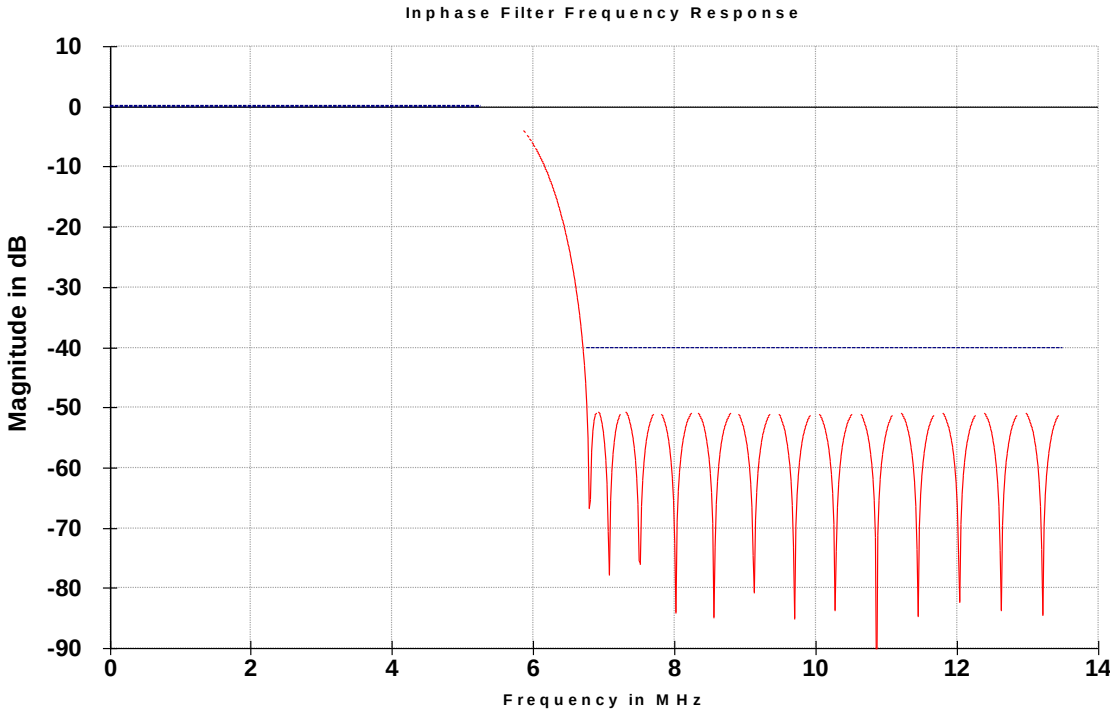

Figure 4 NTSC/PAL Luma interpolation filter (27MHz).

The luma filters for HD operation are shown in Figures 5 to 7.

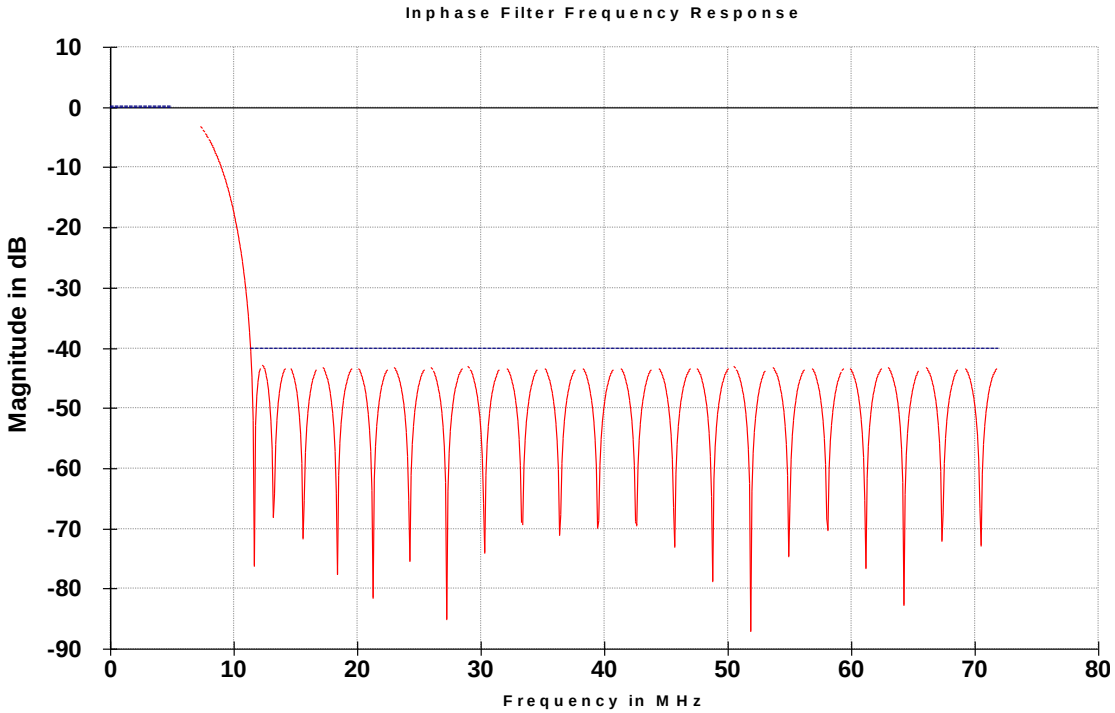

Figure 5 Y interpolator filter response (AHD 720p-25/30Hz).

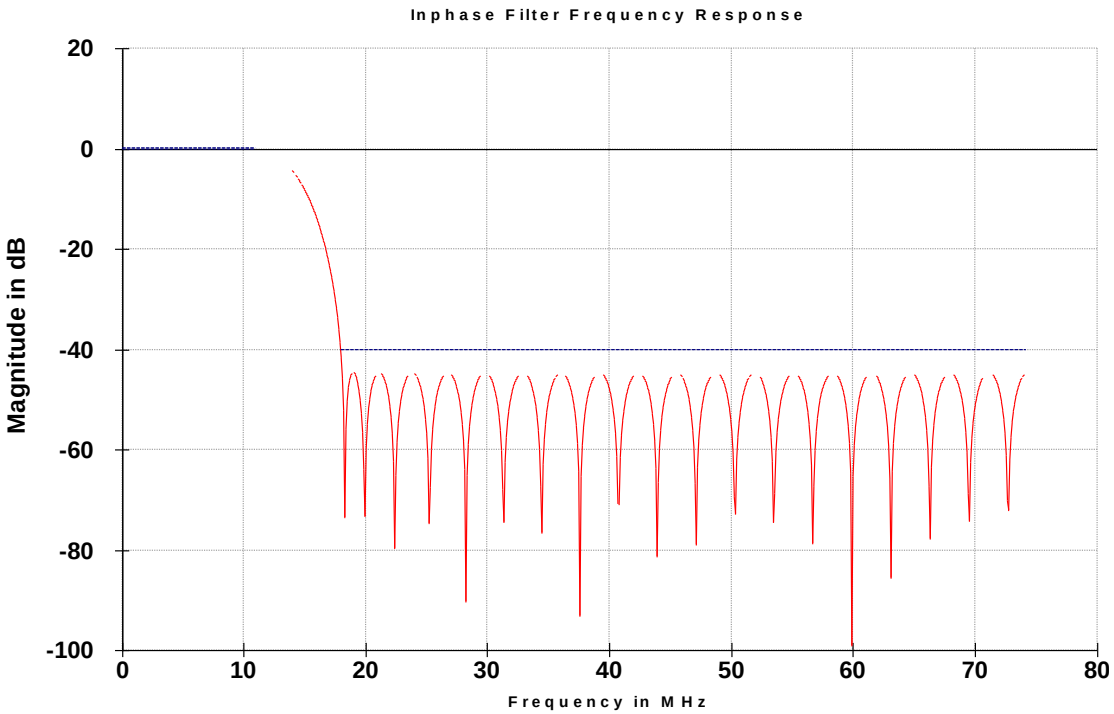

Figure 6 Y interpolator filter response (AHD 1080p-25/30Hz and HD-CVI 720p-25/30Hz).

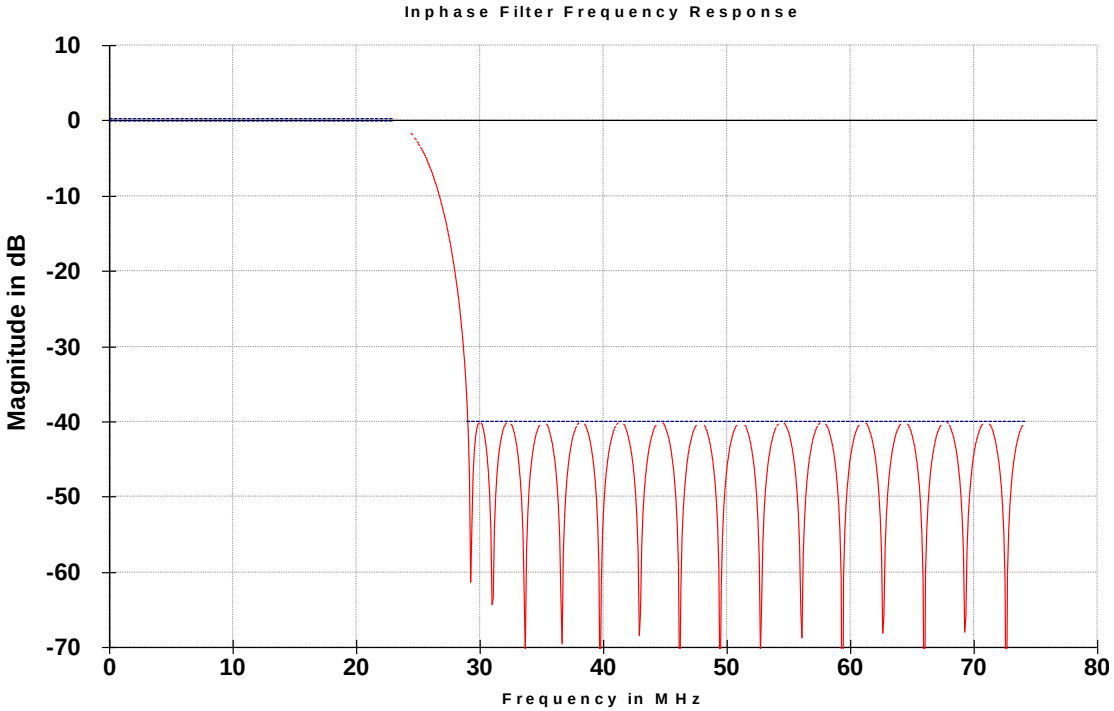

Figure 7 Y interpolator filter response (TVI and HD-CVI 720p-50/60Hz, 1080p-25/30Hz).

The Cb and Cr inputs are conditioned according to the input format applied – see Table 7. The Cb and Cr (chroma) inputs are offset binary with an expected blanking level of 512_{10}. The inputs are latched on the rising edge of the 'Clock' input.

The Cb and Cr inputs are converted to 2's complement format and then interpolated from half 'Clock' frequency (4:2:2 mode) to 'Clock2x' frequency in a 47-tap FIR filter which has an approximate Gaussian response. The appropriate filter is selected automatically based on the standard selected by Control Register 1. For NTSC and PAL operation the chroma filter passband is set at 1.07MHz and the stop band is 3.375MHz – the responses for the three SD supported formats are shown in Figures 8 to 10.

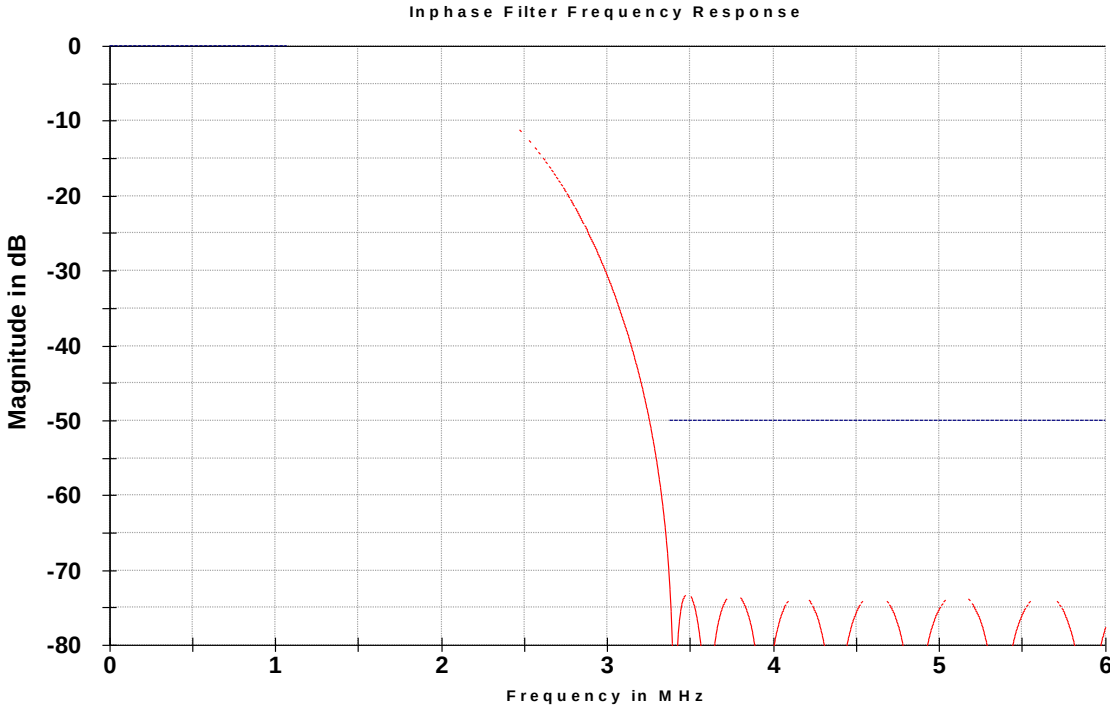

Figure 8 Cb/Cr Interpolation filter response (NTSC/PAL 27MHz).

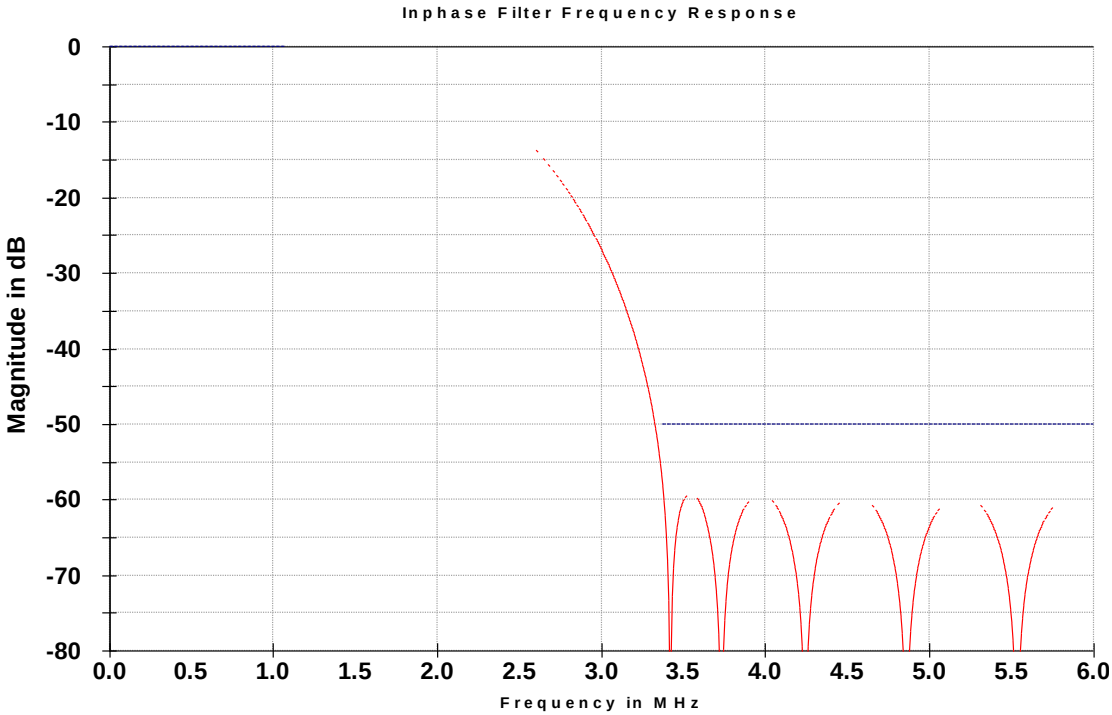

Figure 9 Cb/Cr Interpolation filter response (NTSC/PAL 36MHz).

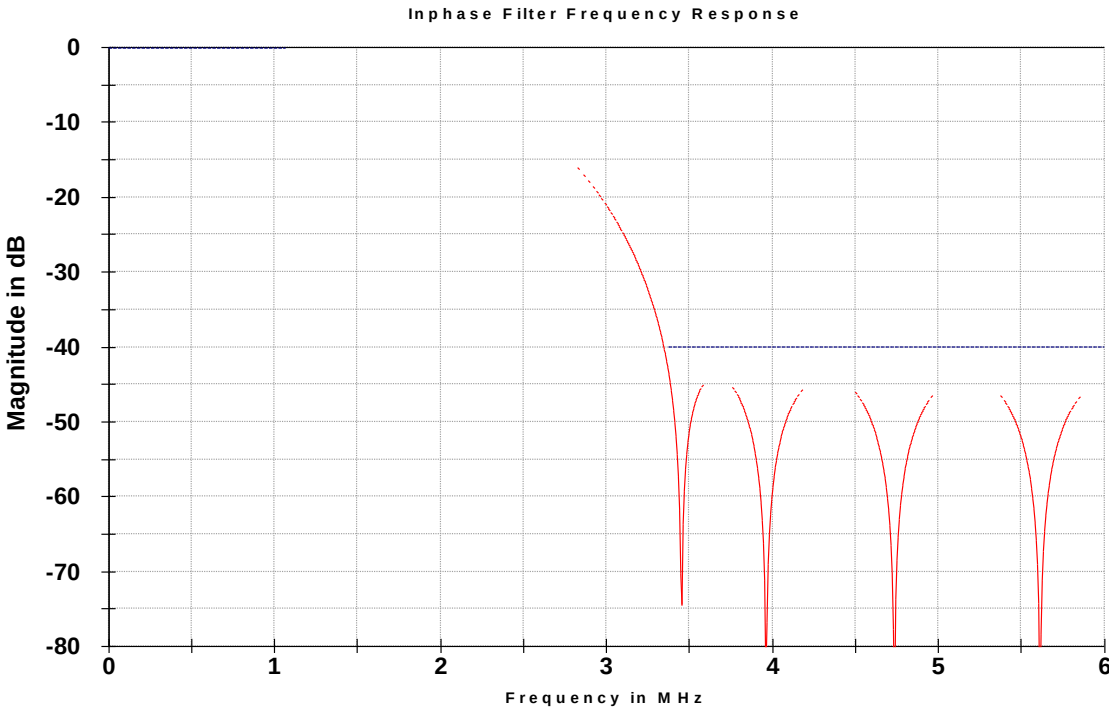

Figure 10 Cb/Cr Interpolation filter response (NTSC/PAL 45MHz).

The filter responses for the HD video formats are shown in Figures 11 and 12.

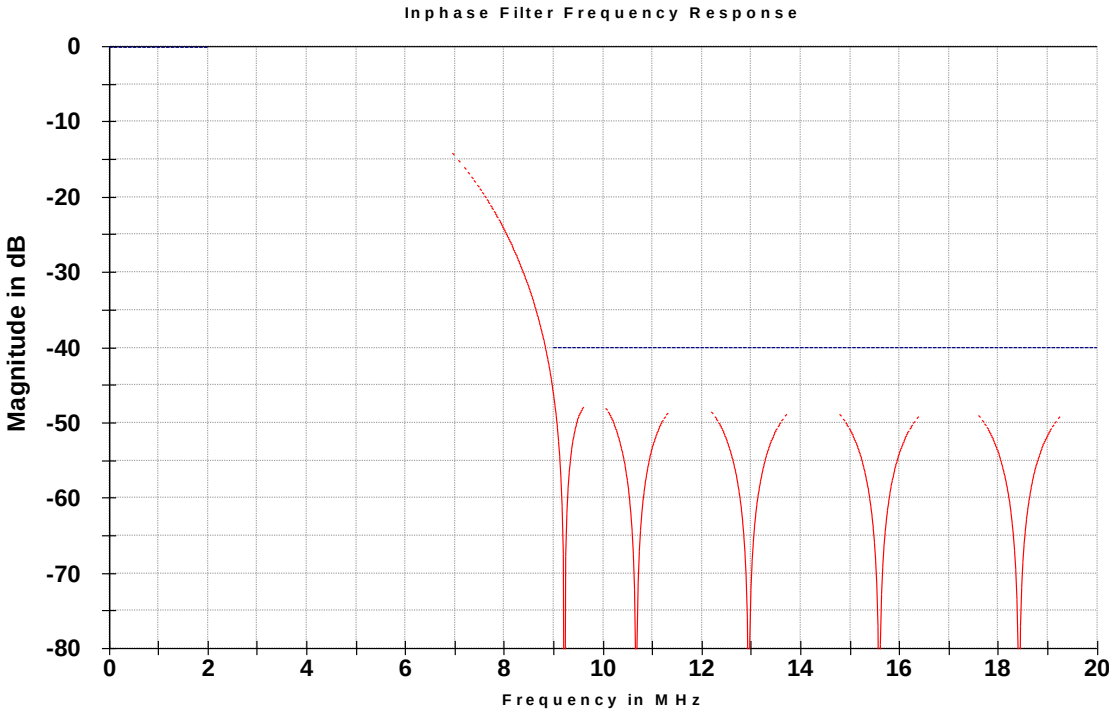

Figure 11 Cb/Cr Interpolation filter response (AHD 720p-25/30Hz).

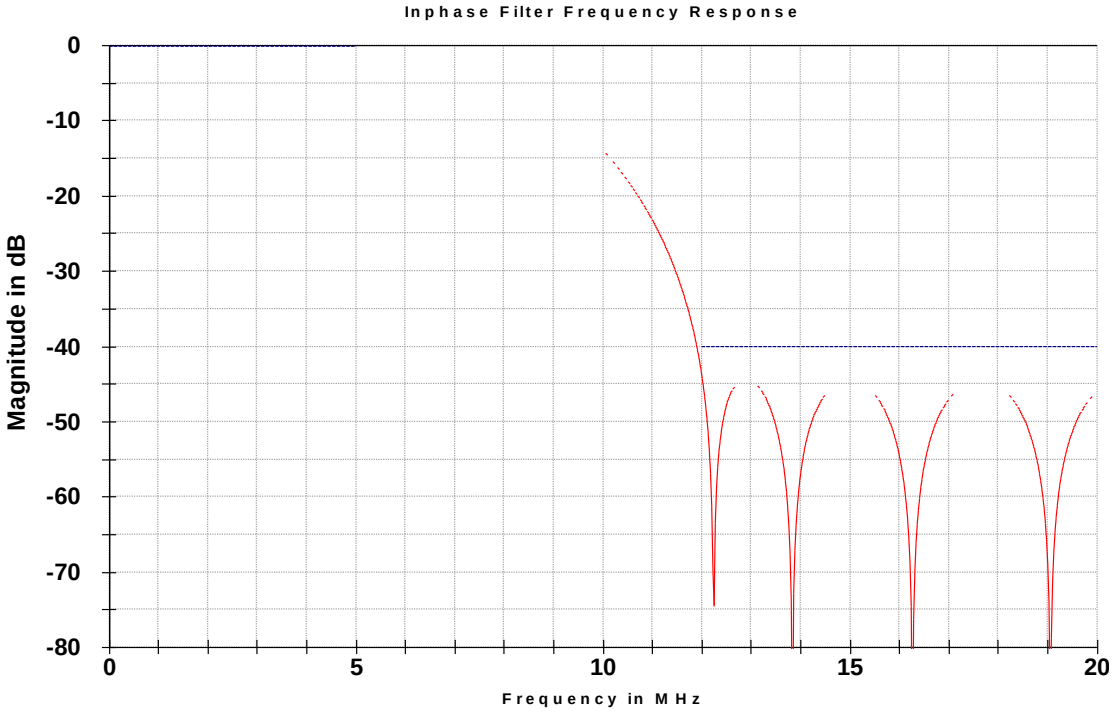

Figure 12 Cb/Cr Interpolation filter response (All other HD standards).

HSync_in (horizontal), VSync_in (vertical field) and FSync_in (vertical frame – if the input is interlaced) signals are used for picture synchronization or, in BT1120 input mode, the embedded TRS timing signals are extracted from the input video data.

The falling edge of the horizontal pulse input is used to reset a 12-bit counter clocked at 'Clock' frequency. This is the 0H reference for the horizontal timing according to the SMPTE specifications and is the mid-point of the analogue tri-level synchronizing pulse. (See Figure 13 for PAL outputs.)

The outputs of this horizontal counter are decoded to produce blanking, synchronization, burst gate and broad pulses. The positions of these pulses are preset according to the selected video standard.

Similarly the falling edge of the vertical pulse input (frame or field depending on whether the input is interlaced or not) is used to reset an 11-bit counter clocked at the beginning of each horizontal line (e.g. a line counter). The outputs from this counter are decoded to produce the vertical sync and blanking pulses. The positions of these pulses are preset according to the selected video standard.

A composite sync pulse is formed from gated combinations of the horizontal, vertical and broad pulses. An analogue version of the digital pulse is also created using a look-up table, giving the edges an approximate raised cosine shape to avoid ringing during the transmission. The 10-90% transition time of the sync edges is approximately 215ns. The amplitude of the sync pulse can be set by Register $08.

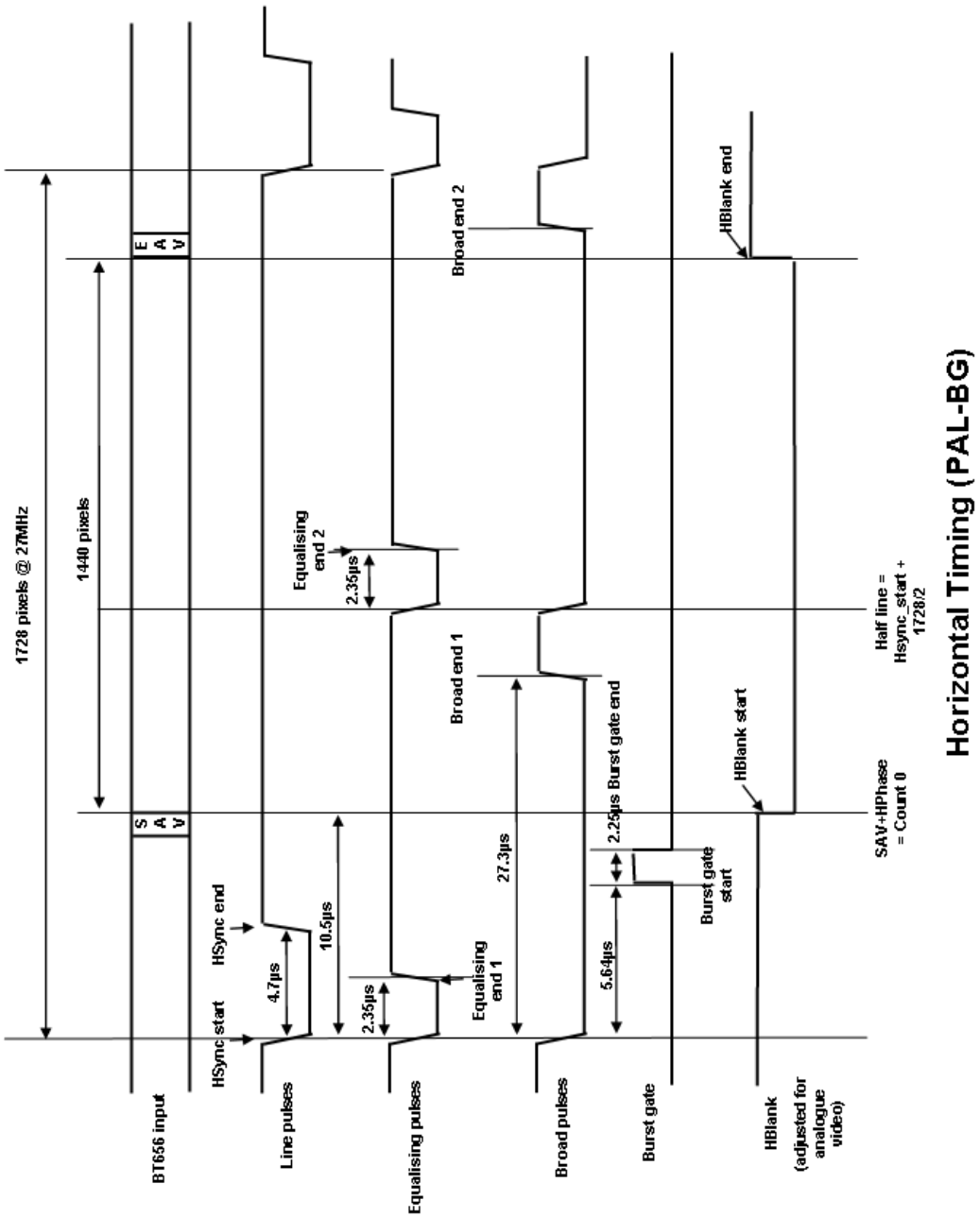

Figure 13 625i input horizontal timing.

Modulator.v

The chroma is frequency modulated onto a carrier, generated using a 32 bit ratio counter clocked from the 'Clock2x' clock. The carrier seed is preset according to the video standard.

$$ratio = \frac{\text{phase change per line}}{\text{pixels per line}} = \frac{F_{sc}}{\text{Clock2x}} = \frac{\Delta\theta_{sc}}{360^\circ} = \frac{\text{subcarrier seed}}{2^{32}}$$

The top 11 bits of this ratio counter (the phase word) are used by the demodulator to generate the sine and cosine waveforms.

The subcarrier phase word is used to address a ROM containing sine and cosine values. A sample of the sine waveform is added, after shaping, to the back porch of the video signal to synchronise the chroma demodulator of the receiver. This colour burst is blanked during the field pulse. The amplitude of the colour burst may be set using Register $0D.

The interpolated Cb and Cr chroma inputs are multiplied by two scaling coefficients (Registers $0B and $0C). These are multiplied in turn by the sine and cosine waveforms. The resulting $U.\sin(2\pi F_{sc}.t)$ and $V.\cos(2\pi F_{sc}.t)$ data is added together to form the final chroma signal which may be programmed in amplitude via Register $0A.

Preemphasis.v

The luma has programmable gain (Register $05) and black level controls (Register $09) applied.
The co-timed luma, sync, chroma and burst are added to create the final composite video output waveform.

A sinx/x filter is applied to the composite signal to compensate for the high frequency sampling losses in the output DAC. The response of the sinx/x filter for HD clock frequencies is shown in Figure 14. The sinx/x filter is a 7 tap FIR filter and may be bypassed using Control Register 2, bit 5.

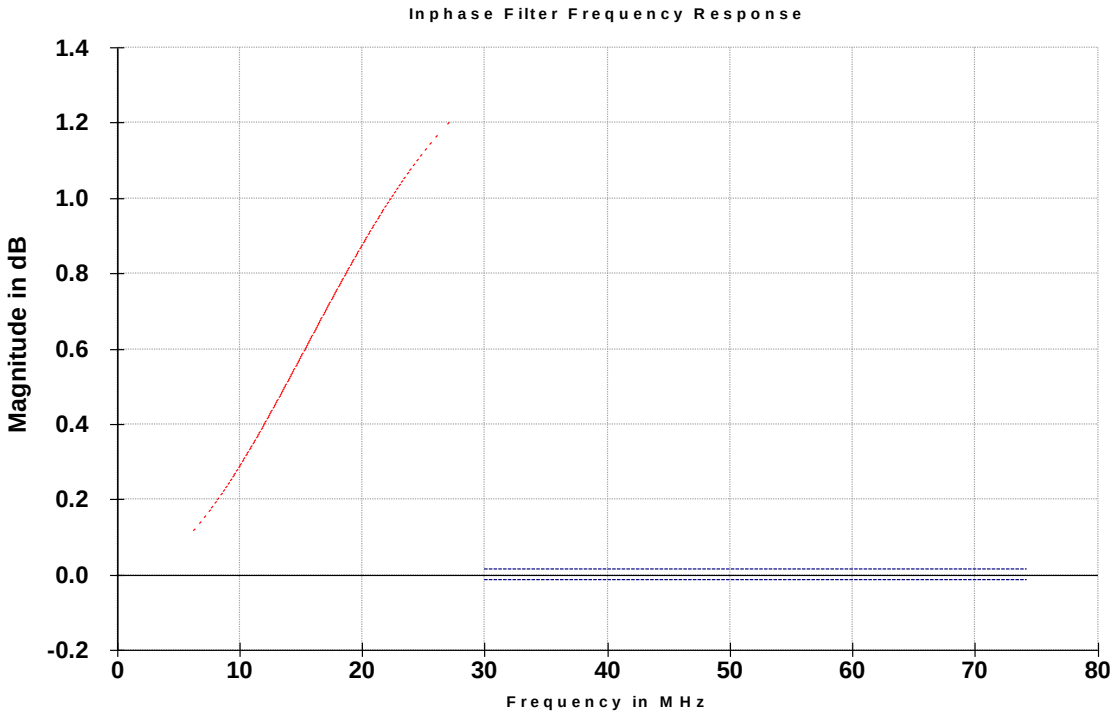

Figure 14 Sinx/x Filter response.

The expected output levels for a 100% colour bar input encoded to PAL is shown if Figure 15.

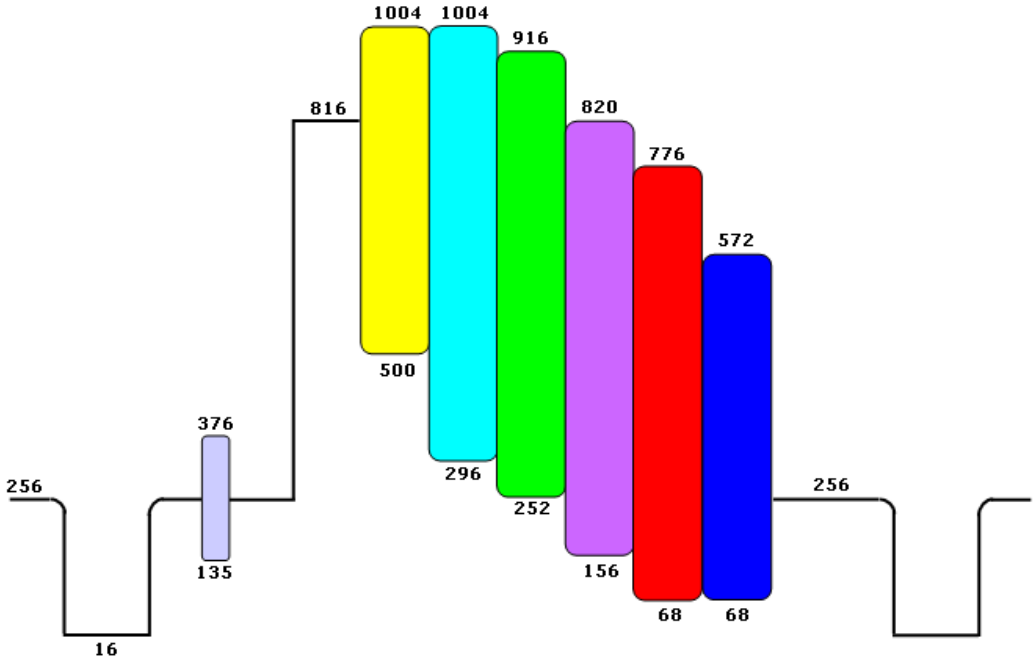

Figure 15 PAL output levels.

6. Register interface

Figure 16 shows the timing diagram for the register interface; it is a conventional microprocessor interface. Each register is selected via a 7-bit address bus. Writes to unused register locations are ignored.

To write to the selected register the PT55_CSn (chip select) input must be asserted low and the A[6:0] register address and the data for this register set up. The PT55_WRn input must then be driven low and high again: On the rising edge of this pulse the data is latched into the address selected. The PT55_CSn input should then be returned high.

For the write to occur reliably the address (A[6:0]) and data (Din[7:0]) must be stable and valid during the low to high transition of the PT55_WRn pulse.

The address input also selects the register data that is presented on the Register_out[7:0] bus. This output is independent of the PT55_CSn or PT55_WRn inputs.

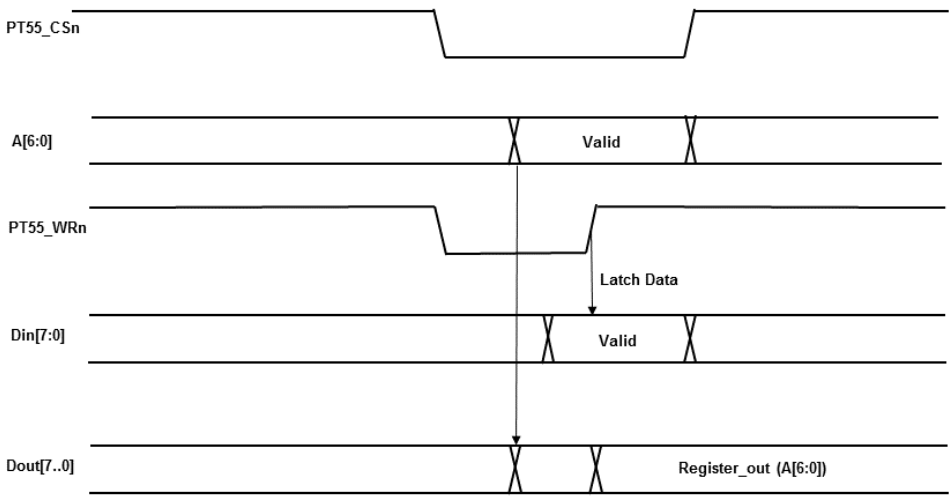

Figure 16 PT55 Register control.

7. Register Descriptions

Table 8 lists all of the control and status registers. All of the registers are 8-bit; unused register bits read back as zeros.

Please note that some registers can be set to values that are illegal and will produce invalid outputs.

Asserting the RESETn input sets the PT55 registers to their default values.

Register Offset	Register Name	R/W	Bit Value	Description					
Control Registers									
$00	**Control 1**	R/W		PT55 control 1 (Video Standard)					
			7:6	HD[1:0]					
			5	S960H					
			4	SD_HDn					
			3:0	Video standard					
				HD1	HD0	S960H	SD_HDn	Video standard	Standard
				0	0	0	1	0000	NTSC-M
				0	0	0	1	0100	PAL
				0	0	1	1	0000	NTSC-960H
				0	0	1	1	0100	PAL-960H
				0	0	1	1	0000	NTSC-1280H
				0	0	1	1	0100	PAL-1280H
				0	0	0	0	0000	720p25 AHD
				0	0	0	0	0001	720p30 AHD
				0	0	0	0	0110	1080p25 AHD
				0	0	0	0	1000	1080p30 AHD
				0	1	0	0	0000	720p25 CVI
				0	1	0	0	0001	720p30 CVI
				0	1	0	0	0110	1080p25 CVI
				0	1	0	0	1000	1080p30 CVI
				1	0	0	0	0000	720p25 TVI
				1	0	0	0	0001	720p30 TVI
				1	0	0	0	0110	1080p25 TVI
				1	0	0	0	1000	1080p30 TVI
$01	**Control 2**	R/W		PT55 Control 2					
			7	Auto Register = '1'. When auto register is set, default values are loaded for each of the standards supported (Control 1, bits 7:0, shaded blue area). If reset then each of the registers are manually loaded. In manual mode, the registers default to the PAL video standard on assertion of RESETn.					
			6	Not used.					
			5	If set to '1' the sinx/x filter is bypassed, else the filter is enabled.					
			4:3	Not used.					
			2:0	Input format			Description (see p.12).		
				001			30 bit separate Y/Cb/Cr, 4:2:2 sampling		
				010			20 bit Y and multiplexed Cb/Cr, 4:2:2 sampling. Demultiplexing using C-enable.		
				011			20 bit Y and multiplexed Cb/Cr, 4:2:2 sampling. Demultiplexing using HSync_in.		
				100			20 bit multiplexed Y/Cb/Cr with embedded sync.		
Video Input									
$05	**Luma_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output Y (luma) component. Value range = $0\text{-}255_{10}$					
$08	**Sync_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output composite sync waveform. Value range = $0\text{-}255_{10}$					

Register Offset	Register Name	R/W	Bit Value	Description
$09	**Black_level**	R/W	7:0	8 bit signed value setting the DC offset value for active video (pedestal). Value range = -128 - $+127_{10}$
$08	**UV_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output chroma amplitude. Value range = $0\text{-}255_{10}$
$08	**Cb_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output Cb chroma component. Value range = $0\text{-}255_{10}$
$08	**Cr_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output Cr chroma component. Value range = $0\text{-}255_{10}$
$08	**Burst_scaling**	R/W	7:0	8 bit unsigned value setting the amplitude of the output colour burst. Value range = $0\text{-}255_{10}$
				SPG
$10	**FSc_1**	R/W	7:0	Subcarrier seed value. 32 bit value = ({FSc_1[7:0], FSc_2[7:0], FSc_3[7:0], FSc_4[7:0]}).
$11	**FSc_2**	R/W	7:0	
$12	**FSc_3**	R/W	7:0	
$13	**FSc_4**	R/W	7:0	
$20	**HPhase_start_1**	R/W	7:0	Horizontal phase control. Sets the delaying between the falling edge of the HSync_in pulse and the 0H horizontal start position. 12 bit word = ({HPhase_start_2[3:0],HPhase_start_1[7:0]}). 1 LSB = 1/Clock µs.
$21	**HPhase_start_2**	R/W	3:0	
$22	**HBlank_start_1**	R/W	7:0	Horizontal blanking start position. 12 bit word = ({HBlank_start_2[3:0],HBlank_start_1[7:0]}). 1 LSB = 1/Clock µs.
$23	**HBlank_start_2**	R/W	3:0	
$24	**HBlank_end_1**	R/W	7:0	Horizontal blanking end position. 12 bit word = ({HBlank_start_2[3:0],HBlank_start_1[7:0]}). 1 LSB = 1/Clock µs.
$25	**HBlank_end_2**	R/W	3:0	
$26	**HSync_start_1**	R/W	7:0	Horizontal sync start position. 12 bit word = ({HSync_start_2[3:0],HSync_start_1[7:0]}). 1 LSB = 1/74.25MHz.
$27	**HSync_start_2**	R/W	3:0	
$28	**HSync_end_1**	R/W	7:0	Horizontal sync end position. 12 bit word = ({HSync_end_2[3:0],HSync_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$29	**HSync_end_2**	R/W	3:0	
$2A	**HBroad1_start_1**	R/W	7:0	Horizontal broad pulse start position. 12 bit word = ({HBroad1_start_2[3:0],HBroad1_start_1[7:0]}). 1 LSB = 1/74.25MHz.
$2B	**HBroad1_start_2**	R/W	3:0	
$2C	**HBroad1_end_1**	R/W	7:0	Horizontal broad pulse end position. 12 bit word = ({HBroad1_end_2[3:0],HBroad1_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$2D	**HBroad1_end_2**	R/W	3:0	
$2E	**HBroad2_start_1**	R/W	7:0	Horizontal broad pulse start position. 12 bit word = ({HBroad2_start_2[3:0],HBroad2_start_1[7:0]}). 1 LSB = 1/74.25MHz.
$2F	**HBroad2_start_2**	R/W	3:0	
$30	**HBroad2_end_1**	R/W	7:0	Horizontal broad pulse end position. 12 bit word = ({HBroad2_end_2[3:0],HBroad2_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$31	**HBroad2_end_2**	R/W	3:0	
$32	**Burstgate_start_1**	R/W	7:0	Burst gate pulse start position. 12 bit word = ({Burstgate_start_2[3:0],Burstgate_start_1[7:0]}). 1 LSB = 1/74.25MHz.
$33	**Burstgate_start_2**	R/W	3:0	
$34	**Burstgate_end_1**	R/W	7:0	Burst gate pulse end position. 12 bit word = ({Burstgate_end_2[3:0],Burstgate_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$35	**Burstgate_end_2**	R/W	3:0	
$36	**Halfline_start_1**	R/W	7:0	Halfline pulse start position. 12 bit word = ({Halfline_start_2[3:0],Halfline_start_1[7:0]}). 1 LSB = 1/74.25MHz.
$37	**Halfline_start_2**	R/W	3:0	
$38	**Equalising1_end_1**	R/W	7:0	Equalising pulse 1 end position. 12 bit word = ({Equalising1_end_2[3:0],Equalising1_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$39	**Equalising1_end_2**	R/W	3:0	
$3A	**Equalising2_end_1**	R/W	7:0	Equalising pulse 2 end position. 12 bit word = ({Equalising2_end_2[3:0],Equalising2_end_1[7:0]}). 1 LSB = 1/74.25MHz.
$3B	**Equalising2_end_2**	R/W	3:0	
$40	**VPhase_start_1**	R/W	7:0	Vertical phase control. Sets the delay between the falling edge of the VSync_in pulse and the 0V vertical start position. 11 bit word = ({VPhase_start_2[2:0],VPhase_start_1[7:0]}). 1 LSB = 1 horizontal line.
$41	**VPhase_start_2**	R/W	2:0	
$42	**VSync1_start_1**	R/W	7:0	Vertical sync pulse start position. 11 bit word = ({VSync1_start_2[2:0],VSync1_start_1[7:0]}). 1 LSB = 1 horizontal line.
$43	**VSync1_start_2**	R/W	2:0	
$44	**VSync1_end_1**	R/W	7:0	Vertical sync 1 pulse end position. 11 bit word = ({VSync1_end_2[2:0],VSync1_end_1[7:0]}). 1 LSB = 1 horizontal line.
$45	**VSync1_end_2**	R/W	2:0	

Register Offset	Register Name	R/W	Bit Value	Description
$46	**VSync2_start_1**	R/W	7:0	Vertical sync 2 pulse start position. 11 bit word = ({VSync2_start_2[2:0],VSync2_start_1[7:0]}). 1 LSB = 1 horizontal line.
$47	**VSync2_start_2**	R/W	2:0	
$48	**VSync2_end_1**	R/W	7:0	Vertical sync pulse end position. 11 bit word = ({VSync1_end_2[2:0],VSync1_end_1[7:0]}). 1 LSB = 1 horizontal line.
$49	**VSync2_end_2**	R/W	2:0	
$4A	**VBlank1_start_1**	R/W	7:0	Vertical blanking 1 start position. 11 bit word = ({VBlank1_start_2[2:0],VBlank1_start_1[7:0]}). 1 LSB = 1 horizontal line.
$4B	**VBlank1_start_2**	R/W	2:0	
$4C	**VBlank1_end_1**	R/W	7:0	Vertical blanking 1 end position. 11 bit word = ({VBlank1_end_2[2:0],VBlank1_end_1[7:0]}). 1 LSB = 1 horizontal line.
$4D	**VBlank1_end_2**	R/W	2:0	
$4E	**VBlank2_start_1**	R/W	7:0	Vertical blanking 2 start position. 11 bit word = ({VBlank2_start_2[2:0],VBlank2_start_1[7:0]}). 1 LSB = 1 horizontal line.
$4F	**VBlank2_start_2**	R/W	2:0	
$50	**VBlank2_end_1**	R/W	7:0	Vertical blanking 2 end position. 11 bit word = ({VBlank2_end_2[2:0],VBlank2_end_1[7:0]}). 1 LSB = 1 horizontal line.
$51	**VBlank2_end_2**	R/W	2:0	

Table 8 Register Descriptions.

8. Output interface

The output of the aCVi encoder is 10-bit, straight binary, video data at 148.5MHz.

This has to be converted to analogue using a digital to analogue converter. On the evaluation board (SM06 revision 0.2) an Analog Devices 10-bit DAC, the AD9705, is used for this purpose.

The FPGA also provides a 148.5MHz clock for the DAC.

The differential analogue outputs from the DAC (1.0V pk-pk) are then amplified by U21 and filtered (U9) to remove clock noise and driven through a cable impedance matching series resistor to the coaxial or twisted-pair cable connectors.

The schematics for this are shown in Figure 17.

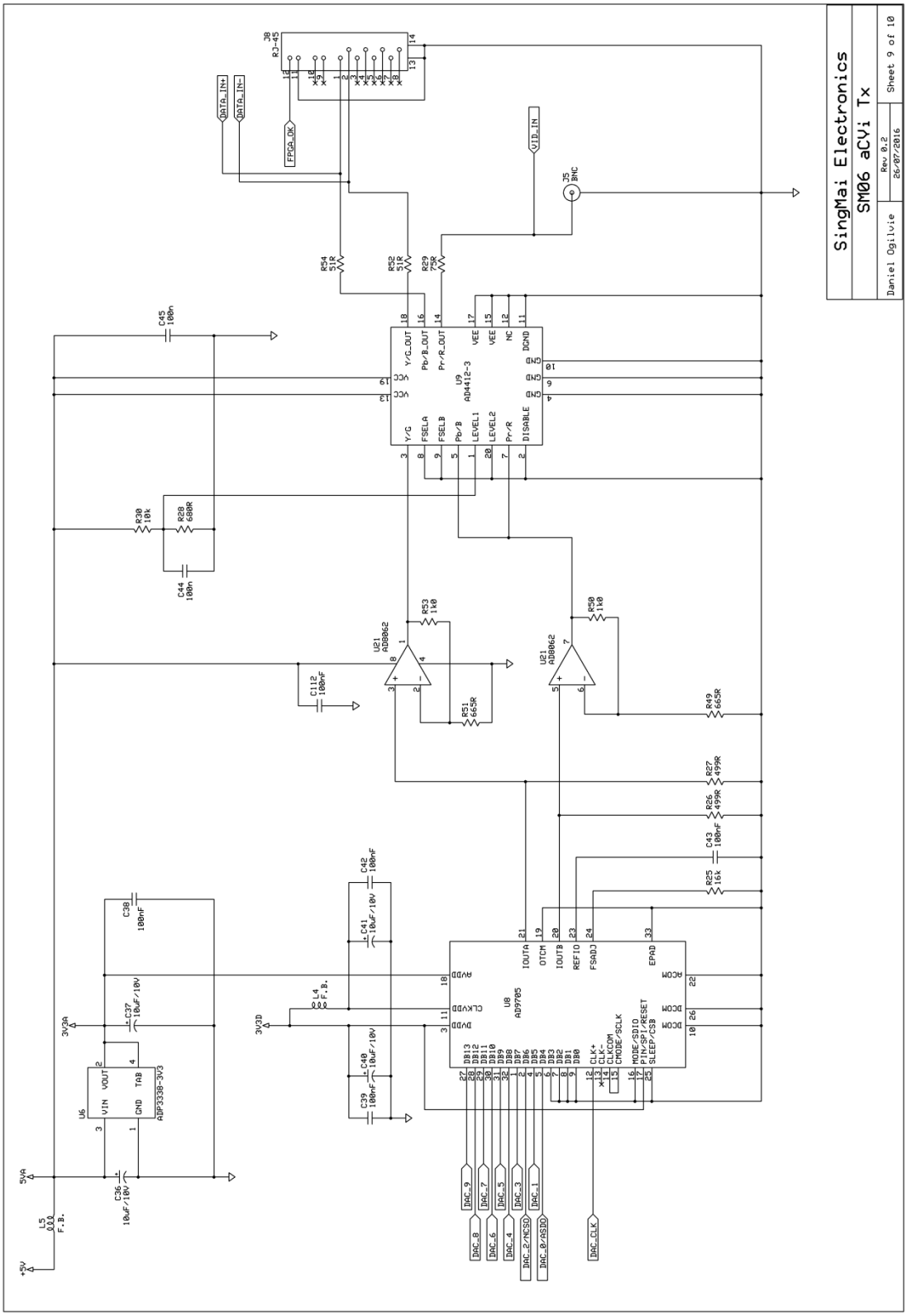

Figure 17 PT55 output interface schematic.