SM03

NTSC/PAL/SECAM

Video Processor and Enhancer

User Manual

Revision 0.1
27th June 2021

Revisions

Date	Revisions	Version
27-06-2021	First draft	0.1

Contents

Figures

1. Introduction

SM03 is a video processor and enhancer for standard definition video (PAL, NTSC and SECAM).

SM03 accepts analogue NTSC-M, PAL or SECAM encoded video which it decodes to a component serial digital interface (SDI) output. Decoding is performed using a proprietary 3D comb filter to maintain the best detail with the lowest artifacts. The video is also retimed in a full frame synchronizer to provide a stable, low jitter output even with out of specification input signals (e.g. from a video cassette player). The video is then passed through a 3D noise reducer and then contrast enhanced and the chroma edge enhanced.

Simple pushbutton control together with an on screen character display allows control of the SM03 parameters.

SM03 requires 5VDC which is provided via the supplied AC-DC converter.

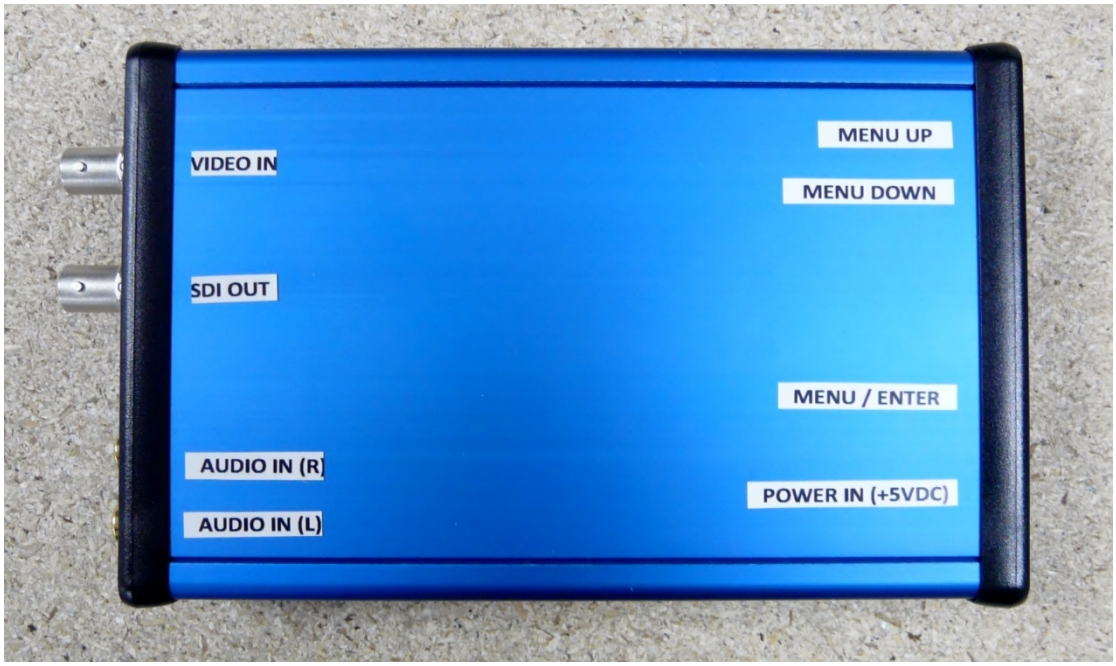

Figure 1 SM03 SD Video processor.

2. Quick start guide

The connections to the SM03 board are shown in Figure 2.

Figure 2 SM03 connections.

The SM03 requires a 5VDC supply which is provided via the supplied AC-DC adaptor. The adaptor accepts AC between 100 and 240VAC – the full specification is provided in Appendix A. The AC-DC adaptor should be supplied with the correct power lead for your country.

Connect the 5VDC jack from the adaptor to the +5VDC 'Power input' socket on the SM03. The yellow 'FPGA OK' LED should light (visible through the Video In BNC) showing the FPGA has been configured successfully.

Connect an NTSC, PAL or SECAM composite video input to the 'CVBS Input' BNC. The SM03 will automatically detect the incoming video standard.

Audio is connected to the SM03 using the two phono (RCA) connectors. The audio is digitized and embedded in the SDI output.

Connect an SDI compatible monitor to the 'SDI out' socket. If you prefer to use an HDMI interface, we recommend the Blackmagic SDI to HDMI converter (see Figure 3) which is available for approximately $50. (https://www.blackmagicdesign.com/products/microconverters)

Figure 3 Blackmagic SDI to HDMI converter.

The default settings for the SM03 are, auto video standard detect, frame synchroniser in ‘normal’ mode, noise reduction on (auto level control), contrast enhance off, chroma enhance on (auto adapt), audio delay = 0ms.

3. SM03 Control

TBD.

Figure 4 Top level SM03 menu options.

4. Comb Filters

At the heart of the SM03 video decoder is a comb filter. This chapter describes the advantages (and disadvantages) of a comb filter.

The analogue television broadcast system (NTSC, PAL or SECAM) was designed as a complete system, from the psycho-visual compromises made at the encoding (camera) end through to the persistence of the phosphor on the cathode ray tube (CRT) in your living room. The advent of large flat screen displays, whilst in many ways being the element that allowed the widespread adoption of high definition television broadcasting, placed additional demands on the analogue video decoder where conventional sources were viewed, and for a large number of viewers that was still the case; that yellow RCA plug was still in widespread use. Even apparent 'HD' (high definition) content can often be up-converted SD (standard definition).

The most obvious result of viewing analogue video sources on a large display is that any artefacts are, of course, larger and visually more apparent. For larger displays the analogue video decoder actually has a more stringent requirement. This problem is compounded because the flat screen displays require additional processing of the analogue source before it can be properly displayed, namely de-interlacing and scaling. The de-interlacer in particular can amplify any artefacts left from the video decoder. This is because the de-interlacer is sensitive to motion in the image and residual artefacts and noise left from the analogue decoder cannot be discriminated from real motion in the image. The result is the de-interlacer may make the wrong mode decision resulting in additional artefacts.

The problem with NTSC and PAL video signals is that, because of the introduction of colour onto a public that had already a large number of monochrome (black and white) TVs, and therefore the introduction had to be without losing compatibility with the old sets. The compromise that was made was to overlay the colour information with the high frequency luma (black and white) information (see Figure 5).

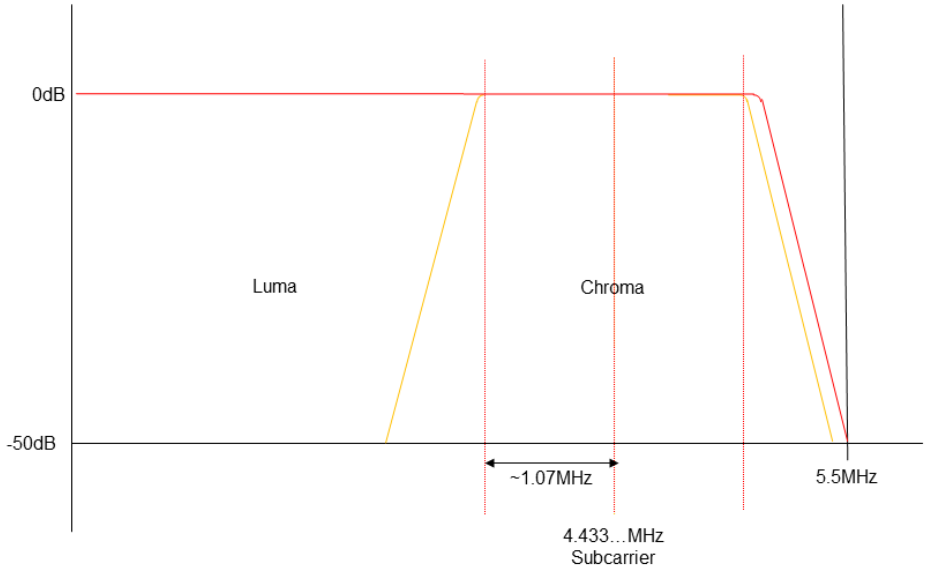

Figure 5 PAL video frequency response.

The simple way to separate the luma and chroma is a low pass filter. All low frequencies (say below 3MHz for PAL) are assumed luma only. All frequencies above 3MHz are assumed to be chroma. The problem with this is we are losing 2.5MHz of luma detail and the video will look 'soft' and lacking in

detail, albeit with no artifacts. The problem is worse for NTSC because the chroma subcarrier is lower, at 3.58MHz.

To separate the high frequency luma from the chroma, the majority of the video decoders use a line comb decoder. The separation relies on the repetitive line to line phase relationship of the colour subcarrier used to encode the chrominance component. For example, for NTSC, each line in the field has a 180° phase shift so adding or subtracting the video signal results in cancellation or reinforcement of the chrominance. That statement is only true, of course, if the colours are of exactly the same hue and even if they are we are not acting upon spatially aligned pixels because not only are we looking at pixels a line apart, but two lines apart because there is the interlaced field line that we do not have access to. Effectively we are looking at pixels 2 lines apart and the situation is worse for PAL because of the additional 90° line based subcarrier phase shift: without specialized and complex processing it is necessary to have a 4 line spacing. Because of all of the above it is necessary to detect when the comb filter will not work, because instead of cancelling the chroma from the luma signal (the cross-colour) we can actually reinforce it (see Figure 6).

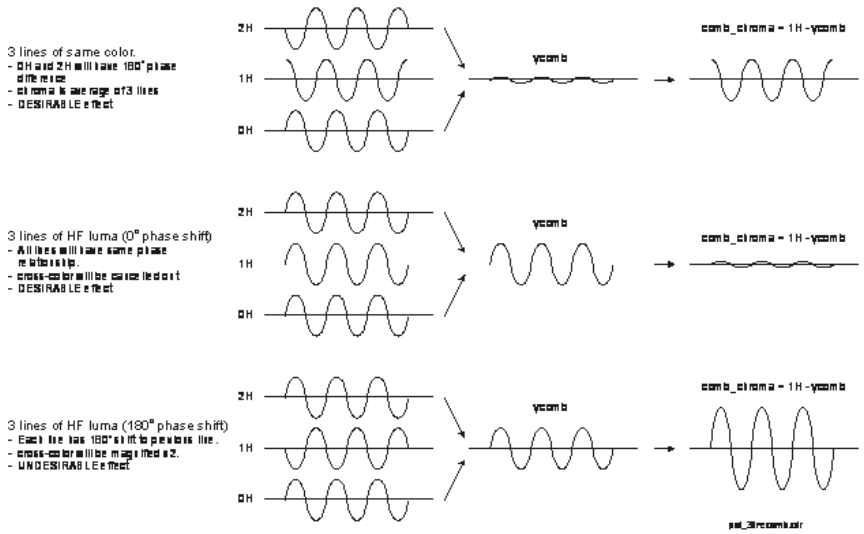

Figure 6 NTSC Comb failures.

It is possible to detect most of the conditions under which a line comb filter based video decoder will fail, and under these circumstances a simple notch filter is usually reverted to, but Figure 1 shows the result of not detecting this condition.

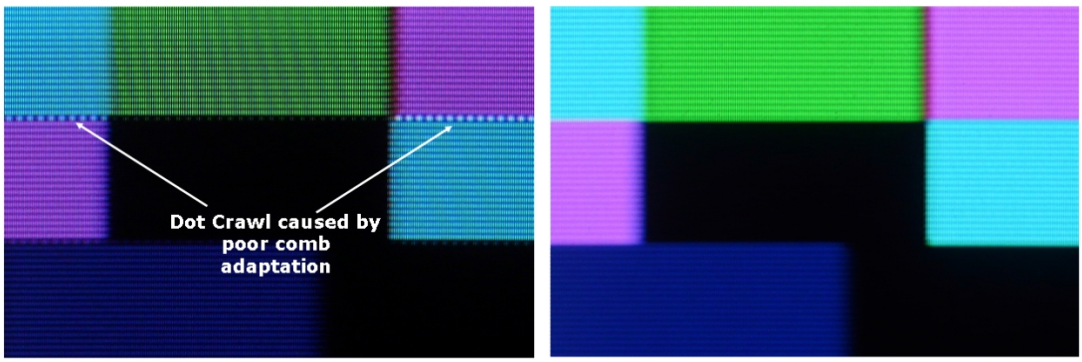

Figure 7 'Dot crawl', left, caused by failing to detect when the comb filter fails.

Although the magenta/cyan boundary seems obvious to the eye, a lot of comb failure detection uses luminance values only to determine the comb mode, and in this case whilst the hues are very different the luminance values are similar so the comb failure is not detected. As mentioned, one of

the issues with these artifacts is that they are not static and cannot be easily removed with further post processing such as noise reduction and because the artefacts are moving they interfere with the motion adaptation of the television de-interlacer.

A similar issue arises if the output of the video decoder is to be compressed as all MPEG compression methods effectively send only the motion of an image. Unable to discriminate between artefacts, video source noise and 'real' image motion it can be shown that up 20% of satellite and cable digital broadcast bandwidth is utilized to send unnecessary information. This is extremely useful bandwidth that is especially useful given the high compression ratios used by today's broadcasters and is the difference between the viewer seeing the highly visible MPEG artefacts such as blocking, or not.

One large improvement to the video decoder that has been made by some manufacturers is to add a 3D comb filter. The filter utilizes the same phase relationship in the subcarrier to cancel the cross-colour as the line comb filter, but a pixel accurate frame delay ensures the pixels are exactly spatially aligned. Even on the most complex images near perfect, artefact free decoding is the result: (I say near perfect because frame combs are very sensitive to clock jitter and clock jitter as little as 1ns over the frame delay period can result in residual subcarrier. PAL also has an addition subcarrier offset which means perfect cancellation cannot occur even with a frame comb).

Figure 8 shows the artefact free image achievable with a well-designed frame comb.

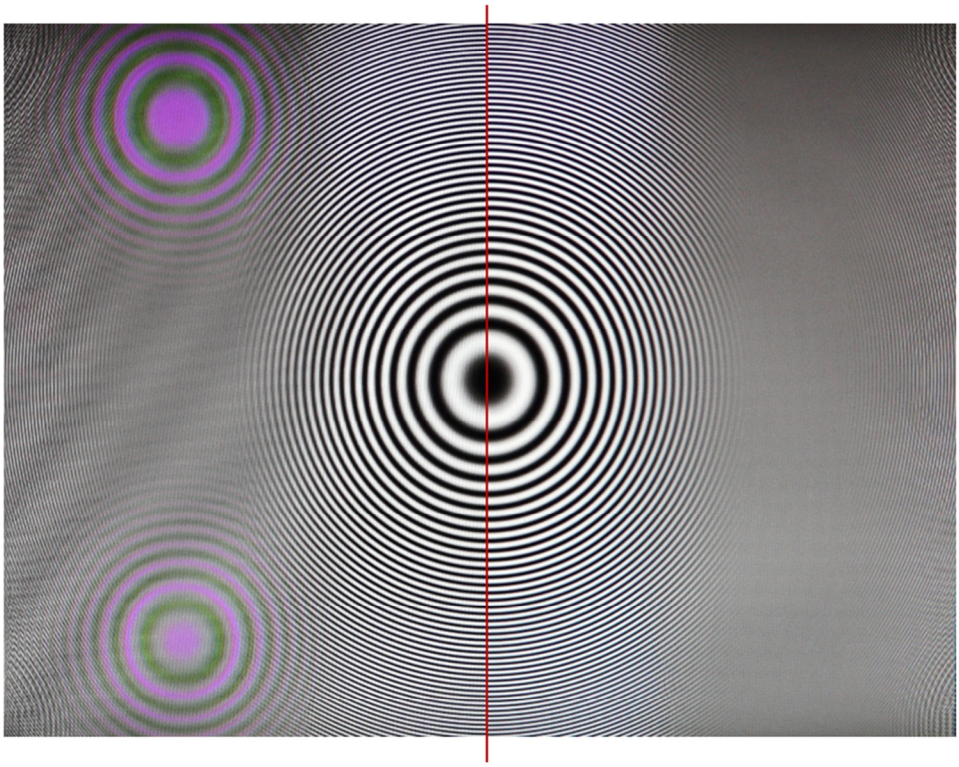

Figure 8 The left image shows a zone plate with a line comb filter. The colours in the image are cross-colour effects caused by the line comb filter no operating correctly. The right side of the image shows the frame comb filter.

The zone plate image in Figure 2 may seem rather esoteric, but you may be more familiar with the shimmering colours created by a newsreader's check shirt, something they seem to have a peculiar penchant for wearing (see Figure 9). Note that because of the fine structure of the check shirt the line comb filter produces, not only artefacts (see the woman's shirt colour) but also a softer image.

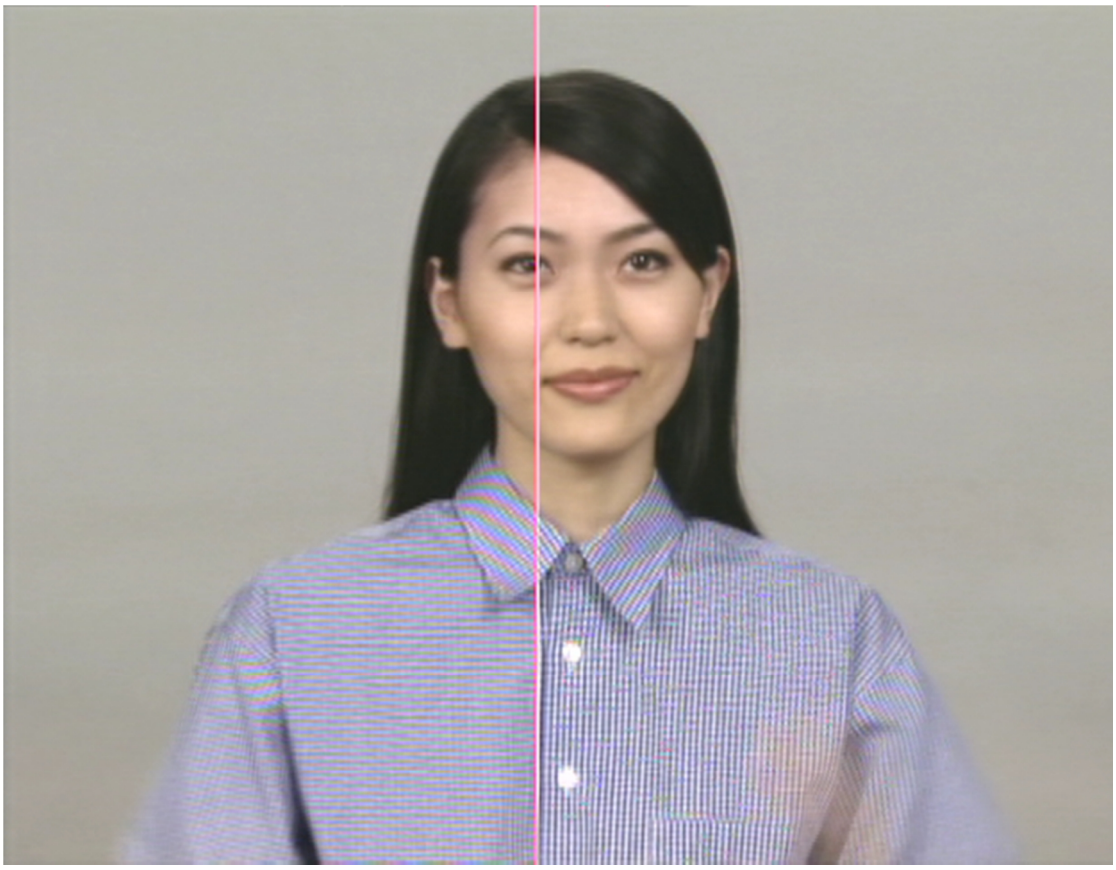

Figure 9 Line comb filter (left): frame comb filter (right).

Another example of the improvement of a frame comb filter over a line comb filter is shown in Figure 10.

Figure 10 Comb filter comparisons.

But of course, the frame comb is not a panacea. We are now looking across comb filter taps of one frame (for NTSC) or 2 frames for PAL, a delay of 80ms in the latter case. Whereas any difference spatially across the 2 or 4 lines caused the line comb filter to fail, now any difference temporally across 33ms or 80ms will cause the frame comb to fail, with similar artefacts being created. The only recourse open to most video decoders is to choose the line comb, or if that is also failing to go to the low pass filter mode, a clean but low bandwidth fall back.

For PAL in particular it can be shown that for a large amount of video material the frame comb cannot be chosen because of image motion; it becomes an expensive luxury, good only for those static demonstration zone plate images. However we have yet one more, under-utilised comb option and that if the field comb. The field comb has an aperture of 262 lines for NTSC and 312 lines for PAL and is therefore much closer spatially than the line comb and closer temporally than the frame comb (especially for PAL).

Figure 11 shows a fast moving still image from the movie Kung Fu Panda. The image is false coloured to show the various comb modes automatically selected by the SM03. The blue colour is the low pass filter mode, and you can see that for the majority of the image, despite the motion, we are able to comb the image in one the three modes the SM03 has available (frame, field and line combs), thereby ensuring the lowest artefacts with the highest resolution. The SM03 constantly monitors each comb filters performance independently and chooses the one with the best performance on a pixel by pixel basis.

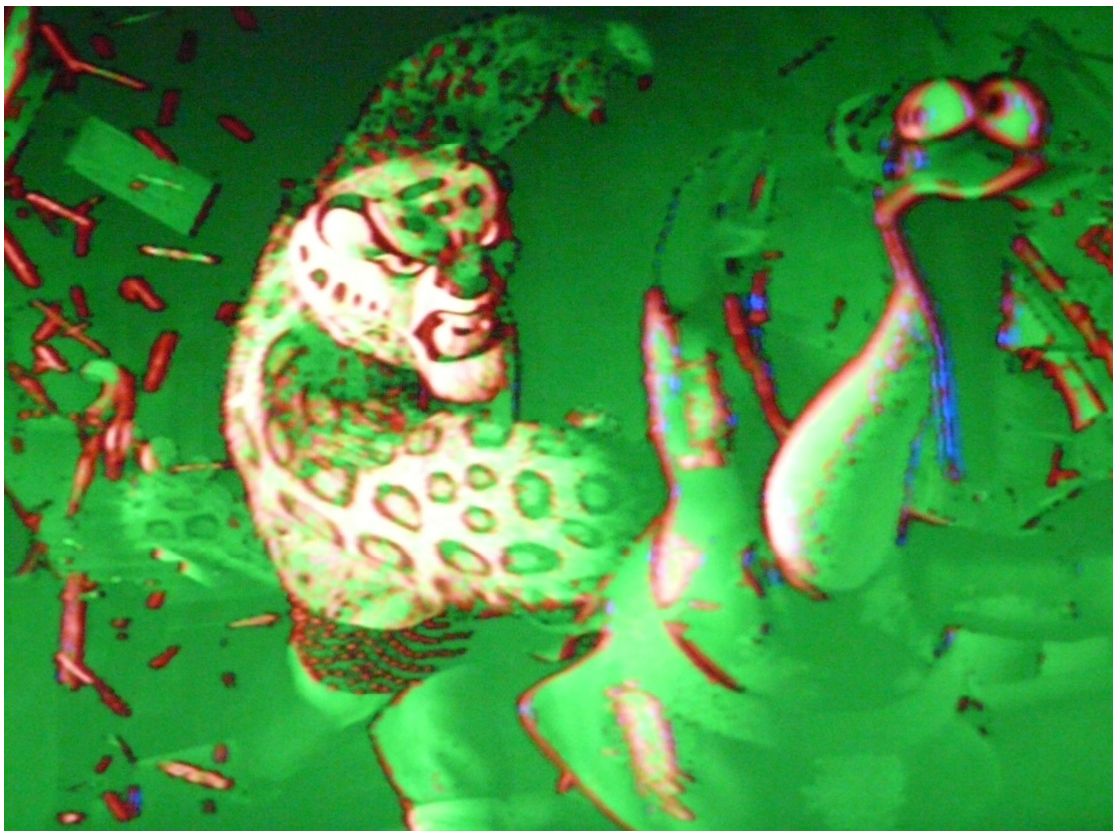

Figure 11 Comb failure detection.

Figure 3 Comb Modes: Green = frame comb, Magenta = field comb, Red = line comb/notch filter.

To avoid a complex memory architecture it is also possible to forgo the usual symmetrical architecture employed in 3D comb filters where the frame before and after is available to the filter. An asymmetric comb filter where only the past frame (or field) tap is available can yield similar

results, simplify the memory interface and allow the design of a video decoder with minimal delay. Another advantage of this architecture is that no corresponding audio delay need be employed to prevent lip-sync issues (the audio and the video being mistimed).

5. Video Noise reduction

A simplified block diagram of the SM03 video noise reducer is shown in Figure 4.

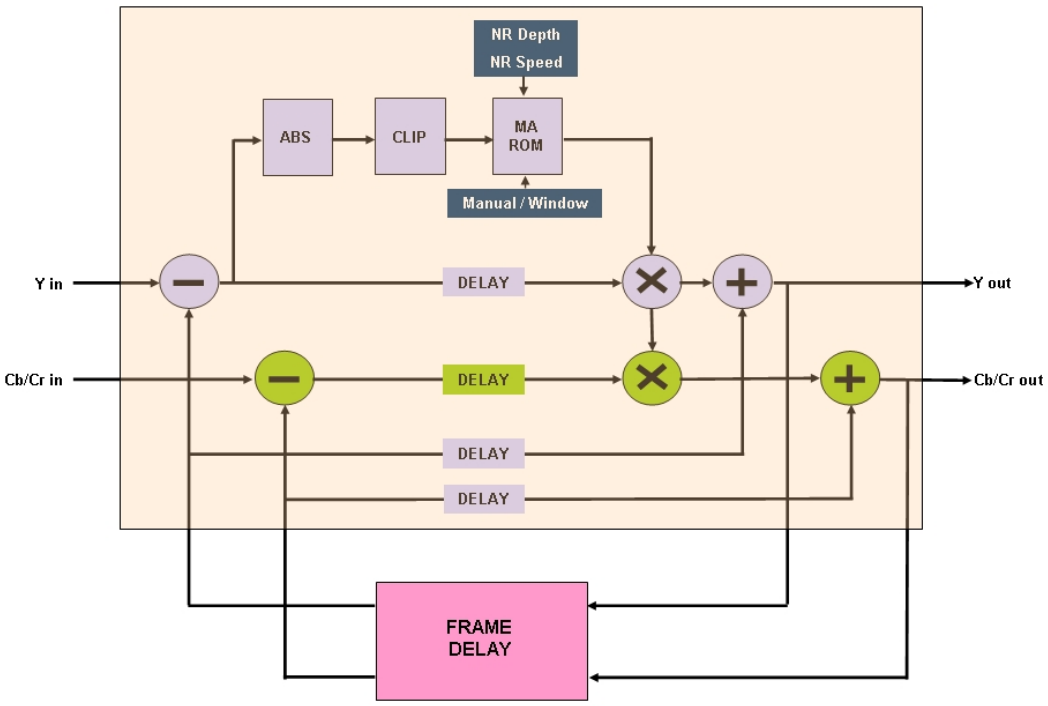

Figure 12 Video noise reducer block diagram.

This noise reducer architecture is a rearrangement of the following equation:

$Y_{out} = k*Y_{in} + (1-k)*Y_{delay}$ where:

Y_{out} is the output luma (or Cb/Cr output)
Y_{in} is the input luma (or Cb/Cr input)
Y_{delay} is the output from the frame delay
k is the feedback factor.

The k factor sets the degree of noise reduction. However temporal noise reduction such as this leaves trails on moving objects. To prevent this the frame difference from the first subtractor (Y channel only) is used to detect motion and reduce the noise reduction where motion occurs.

The absolute value of the difference is calculated and this value is then clipped, (all differences above value 127 are clipped to 127). The clipped differences value is then used to address a lookup table along with two controls, the depth and the speed. These fixed controls (via control register 1) are used to set the degree of noise reduction (NR_Ydepth[1:0] and NR_Cdepth[1:0]) and the speed that the noise reducer responds to motion (NR_speed[2:0] - the level of the difference value that starts a reduction in the noise reduction. Two lookup tables are used, one for the Y value and one for the Cb/Cr values because the chroma trails are less visible to the eye so a higher degree of noise reduction may be applied to them.

The LUT adaptation values are shown graphically in Figures 13 and 14. The degree of noise reduction is shown on the vertical axis (value 1 is no noise reduction) and the horizontal axis if the value of the luma difference. So, for example, with no motion (difference value = 0) the k value is set to 0.3, 0.5 or 0.7 depending on the depth control register setting. As the difference value increases then. Depending on the NR_speed setting (either value 24, 32, 40, 48, 56, 60, 72 or 80) the k value is then adjusted according to the curves shown in the diagram. An NR_speed setting of '111' (80) is the slowest to adapt to motion and the value '000' (24) is the fastest to adapt to motion.

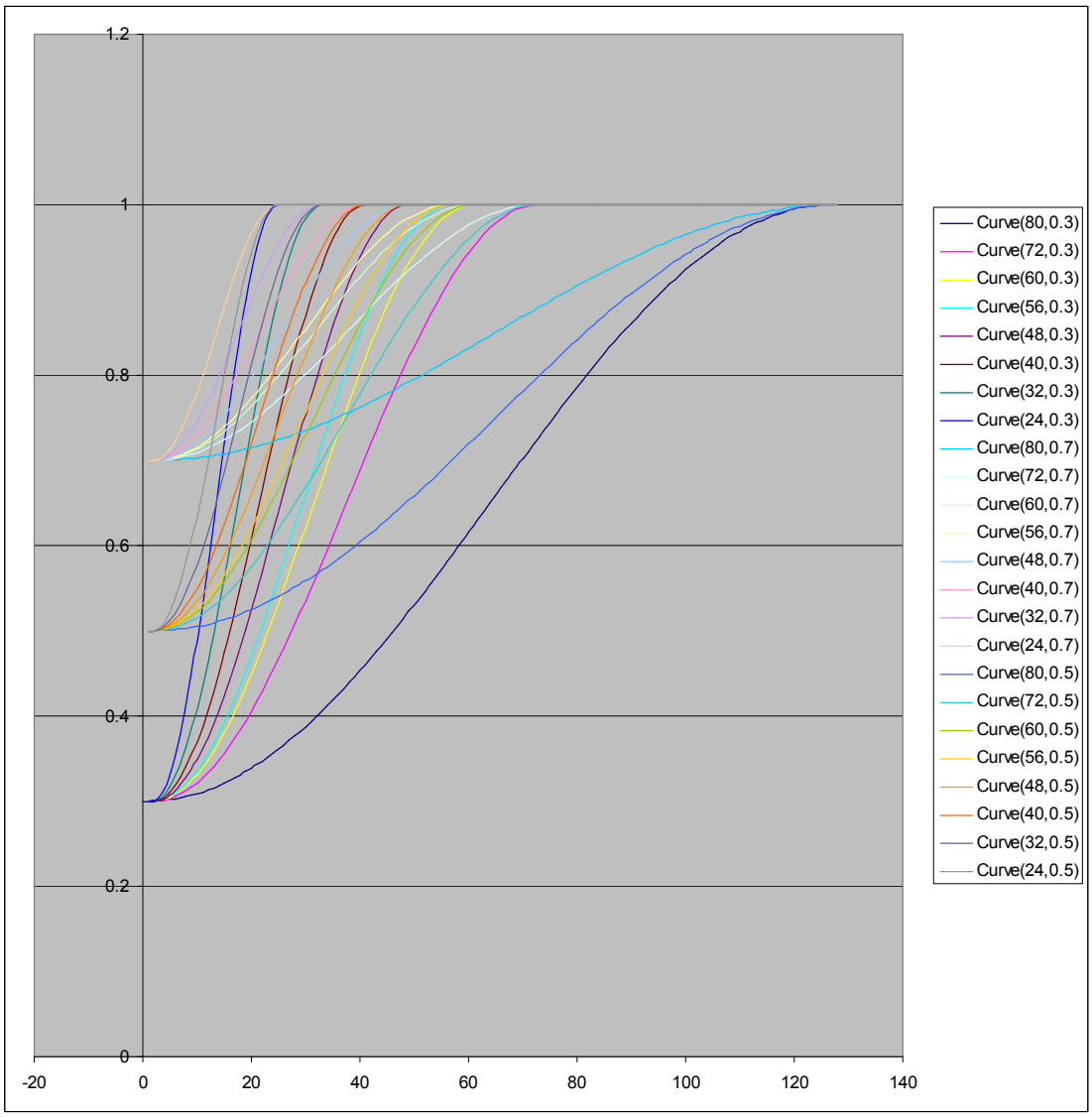

Figure 13 Y (Luma) channel noise reduction adaptation tables

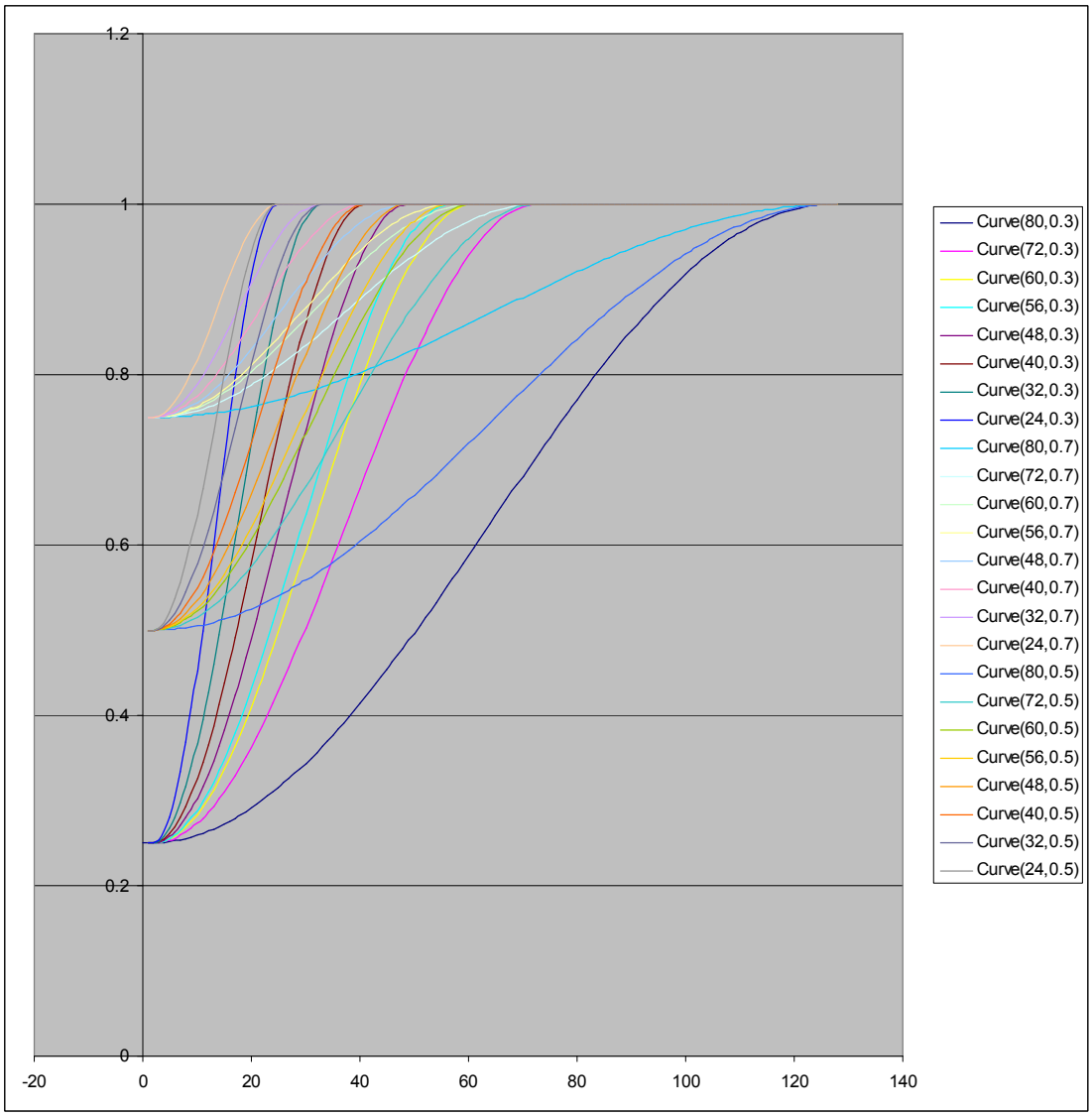

Figure 14 C (Chroma) noise reduction adaptation values.

The expected degree of noise reduction (Gaussian noise) for static objects is 4.8dB (k=0.5), 8.5dB (k-0.25) and 11.8dB (k=0.125).

For conditions where the noise is very high and the motion adaptation is not required a manual k factor may be chosen (see Figure 15, a screen capture of an image-intensified – night vision - camera).

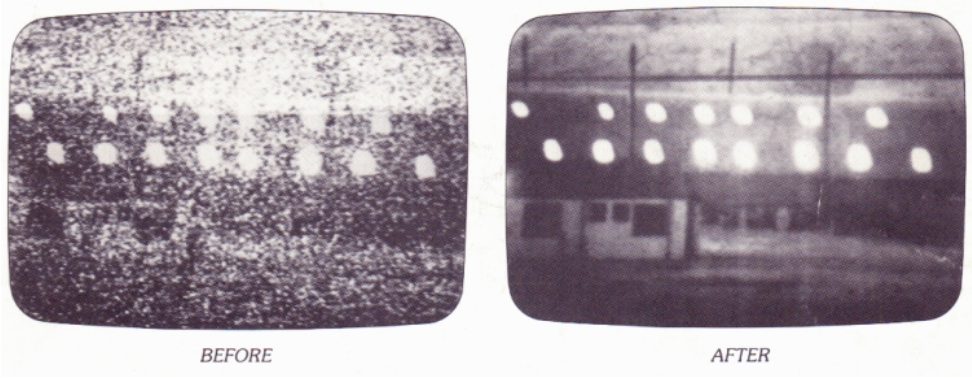

Figure 15 SM03 noise reduction - image intensified camera.

6. Technical Overview

Figures 16-25 show the schematics for the SM03. Below is a brief technical description of the module.

Sheet 1.
J2 is the 5VDC power input connector to the SM03 module. The 5VDC is protected from reverse polarity and over-range inputs by D5, D6 and the resettable fuse, F1. The input is then filtered by L5 and C31/C32 to provide the 'clean' 5VDC for the analogue output stage and also regulated by switched mode regulator U5 to provide the 3.3VDC supply voltage.

Sheet 2.
U7 provides the 1.2VDC for the internal voltage of the FPGA. U9 provides the 2.5VDC for the analogue PLL circuity of the FPGA and L7 and C115 filter the VCCINT for the FPGA PLL digital blocks. U6 provides the 2.5V for the FIFO memories. U8 provides a power on reset for the FPGA.

Sheet 3.
J5 is the CVBS video input. It is pseudo differentially received to reduce any hum pickup and converted to a single ended signal by U17. U18 provides an anti-aliasing filter. The requirements for the anti-aliasing filter are relaxed by over-clocking the ADC at 54MHz. The first stage of the SM03 decoder decimates this to allow the SM03 to then be clocked at 27MHz.

U20 and D10 provide a sync tip clamp which clamps the most negative part of the input video (the sync tip) to the bottom reference of the ADC. U19 provides a 2.5V reference voltage for the front end. U21 is the ADC which, as mentioned, is clocked at 54MHz. The ADC provides the straight binary, 12-bit, digital composite data to the FPGA and the SM03 for decoding.

Sheet 4.
U1 is the FPGA. The FPGA is an Altera E3C40 device in a 240 pin 0.5mm PQFP package. The FPGA contains the PT5 video encoder, the SDRAM controller, the frame synchronizer control, a SingMai PT13 control microprocessor, a colour bar generator and the BT656 formatter.

Full details for the PT5 video decoder may be found here:
https://www.singmai.com/IP_Cores/PT5.html

Sheet 5.
The FPGA is a volatile device and needs configuring on switch on, which it does using U15, a 16Mb EEPROM. The device is automatically configured on switch on, and successful configuration is indicated by LED D9, 'FPGA OK'. The EEPROM may also be reprogrammed via J4, which is compatible with the Altera 'USB-Blaster' and the Quartus Programmer. J3 allows the FPGA to be reprogrammed temporarily using the JTAG interface.

Sheet 6.
U11 and U12 provide 16Mb x 32 of SDRAM which is used for the 3D comb filter. The controller for the SDRAM is in the FPGA.

Sheet 7 and Sheet 8.
U2 and U3 are the FIFO memories. They are organized as 20 bit wide, 4:2:2 format and are written with the timing signals from the decoder and read out with an independent, asynchronous, crystal controlled sync pulse generator to ensure stable outputs regardless of the input video.

Sheet 9.
U4 is the SDI transmitter. It accepts BT656 format video (10 bit) from the FPGA (synchronizer output) and formats it to an SMPTE-259M compatible output (J1).

Sheet 10.

X4 provides a stable 27MHz for the output sync pulse generator.
SW1-3 provide for control of the SM03.
U22 is a I2C controlled EEPROM that can be used to store parameters.

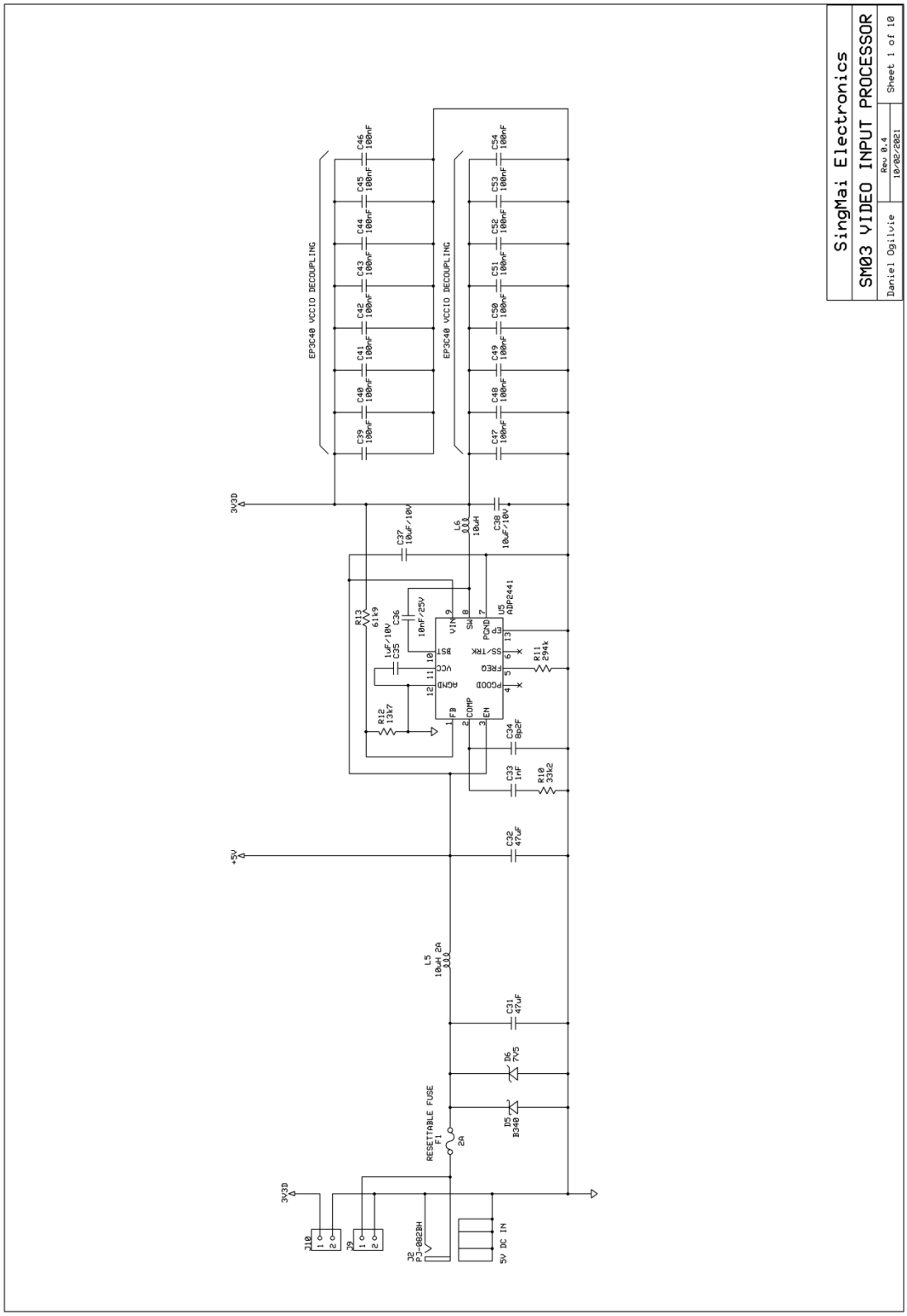

Figure 16 SM03 schematics- Sheet 1.

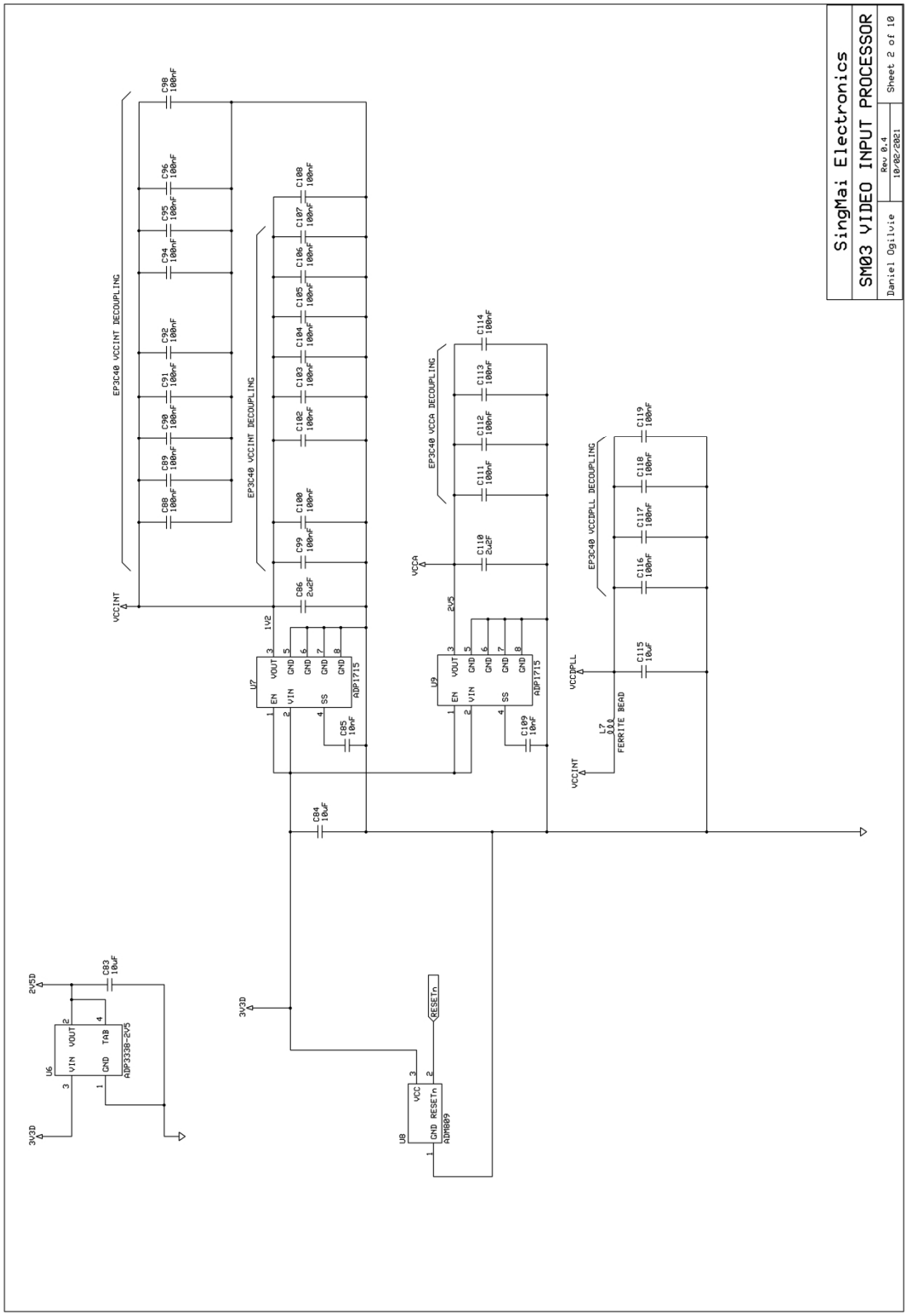

Figure 17 SM03 schematics- Sheet 2.

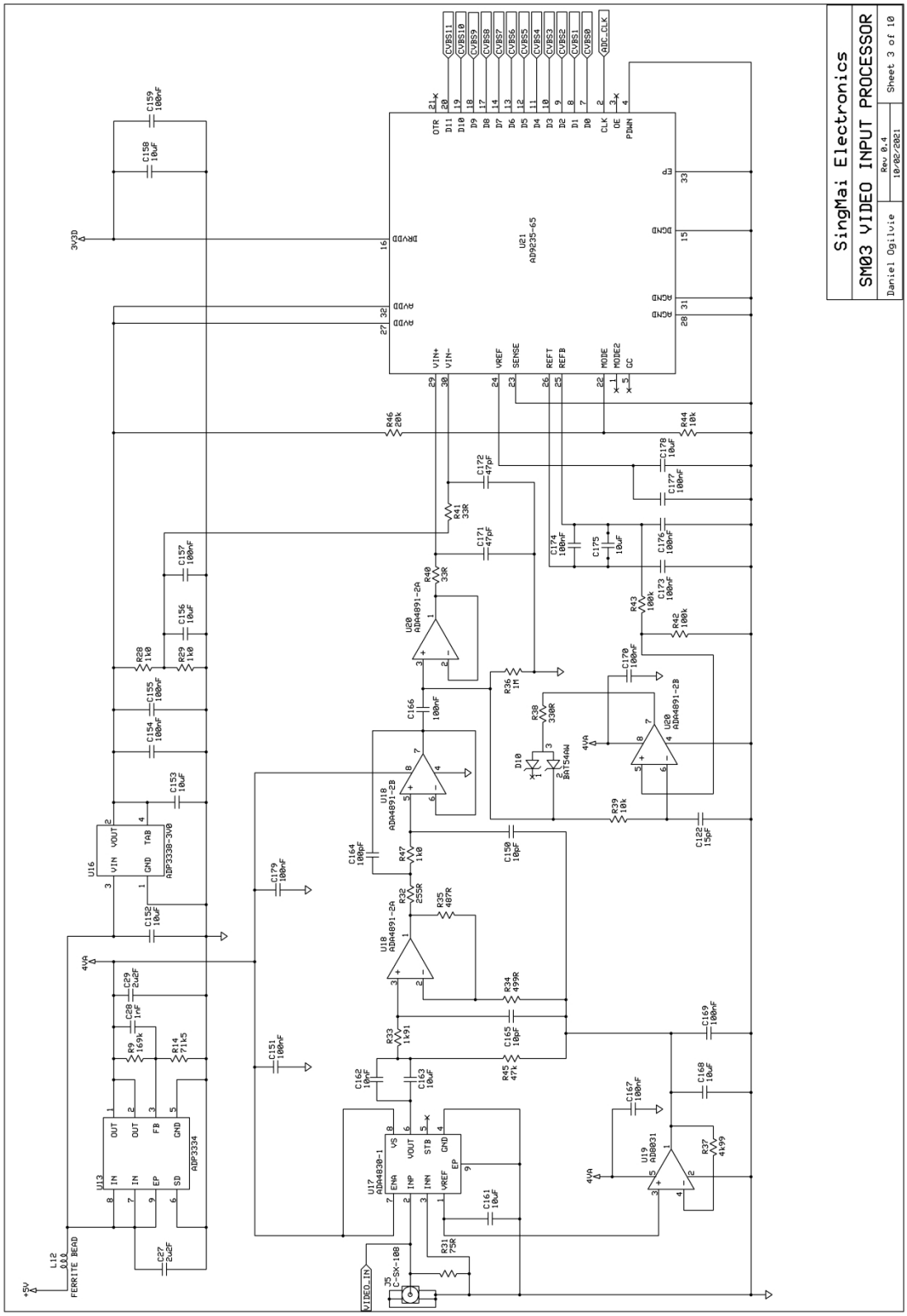

Figure 18 SM03 schematics- Sheet 3.

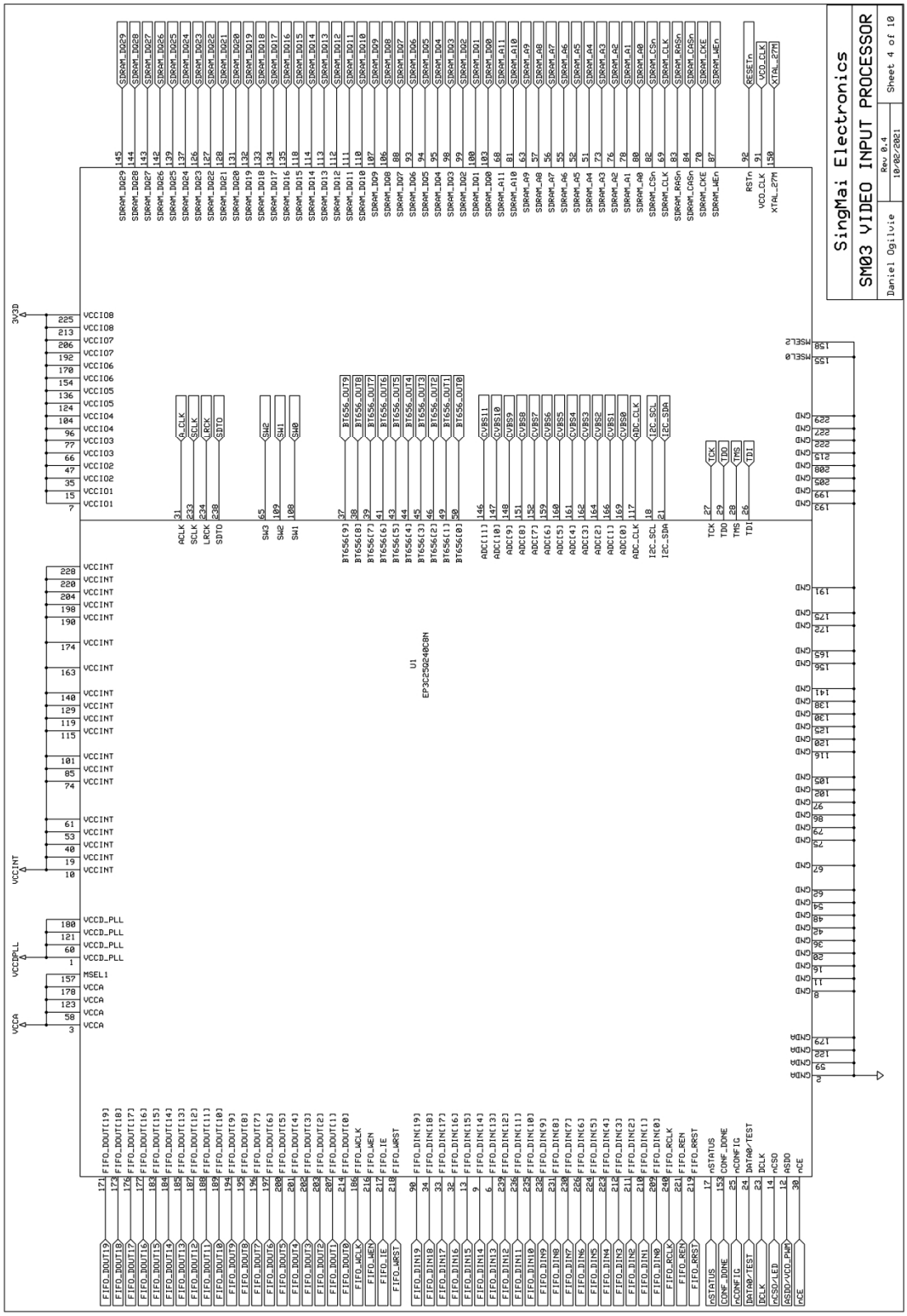

Figure 19 SM03 schematics- Sheet 4.

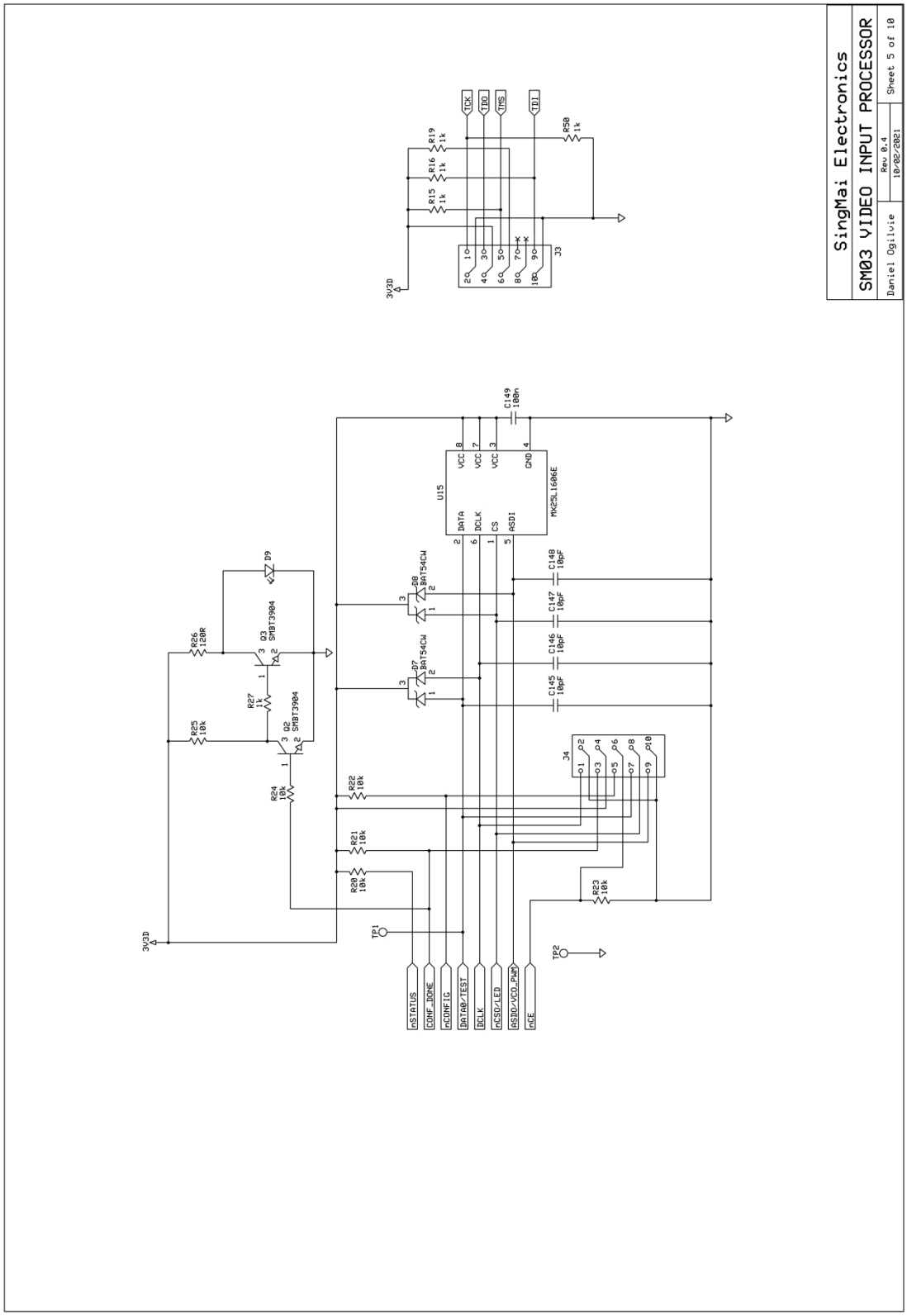

Figure 20 SM03 schematics- Sheet 5.

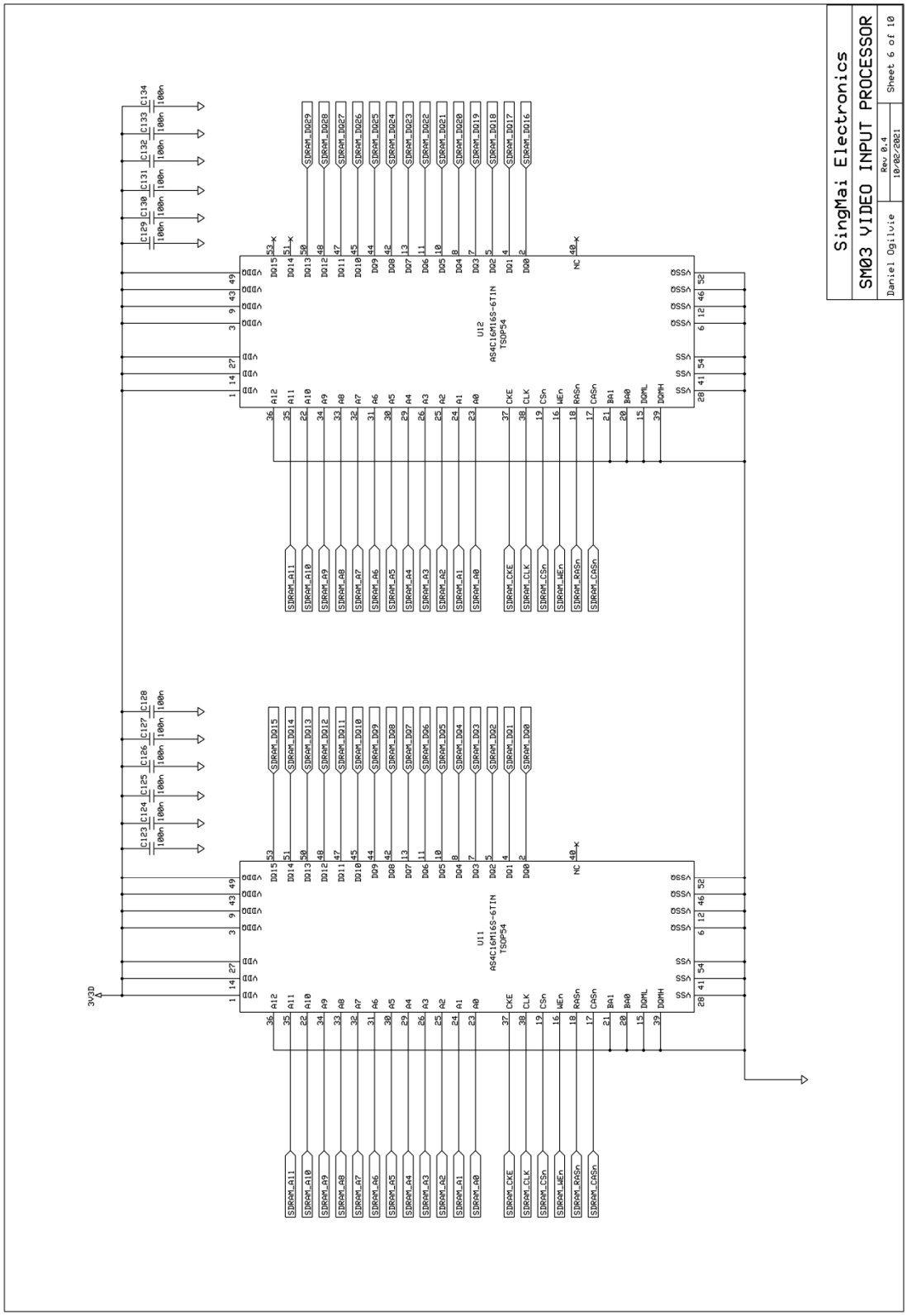

Figure 21 SM03 schematics- Sheet 6.

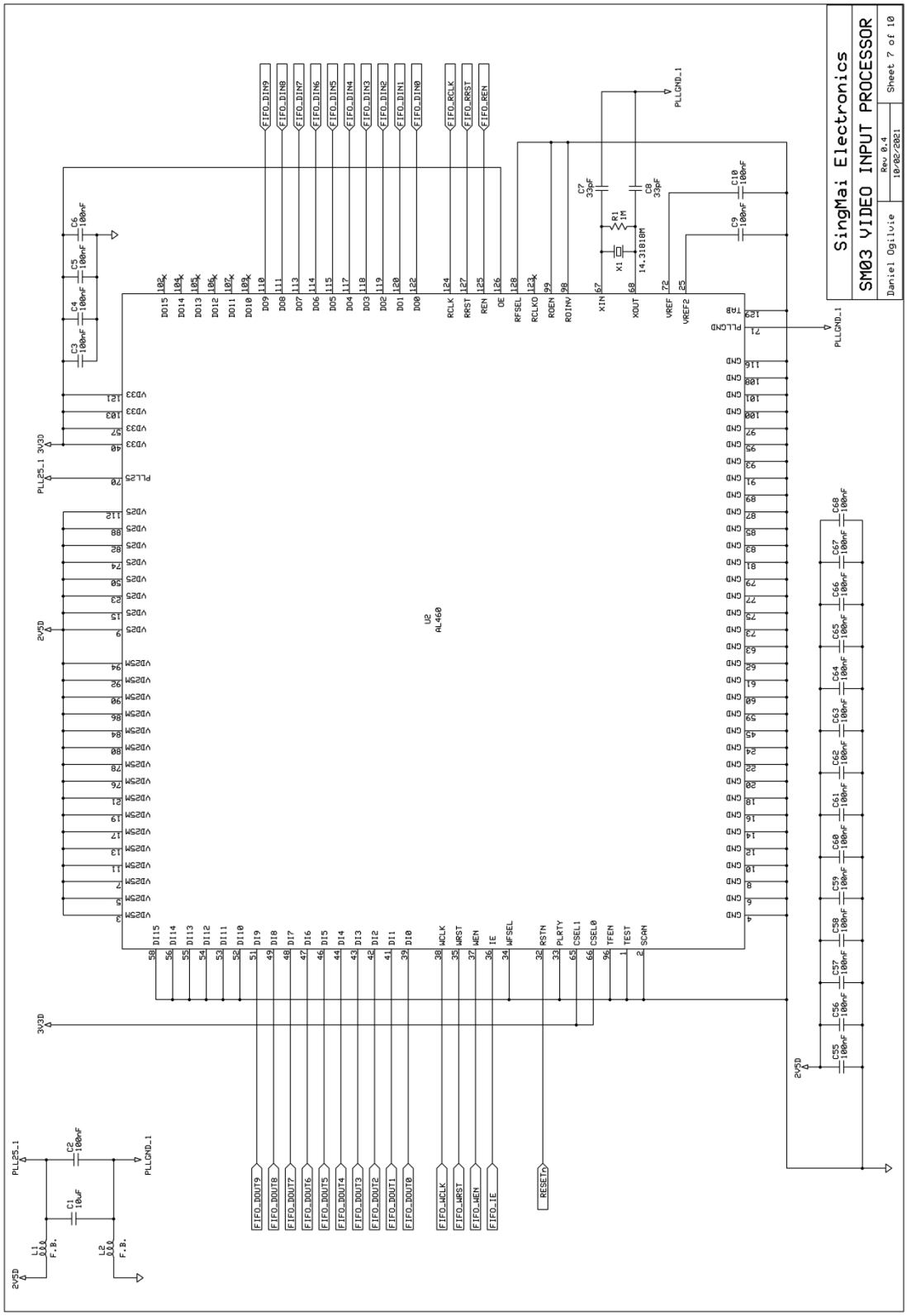

Figure 22 SM03 schematics- Sheet 7

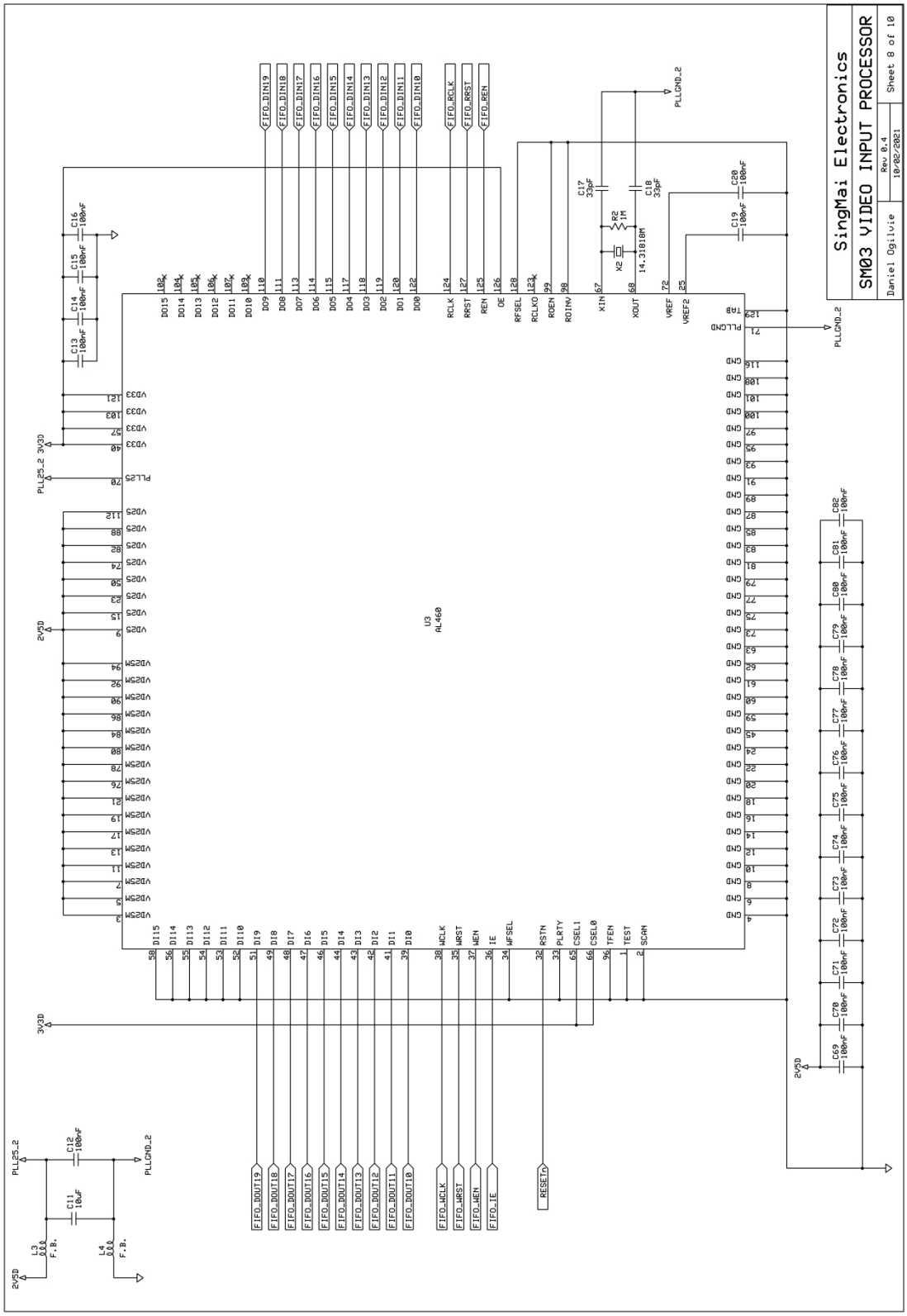

Figure 23 SM03 schematics- Sheet 8.

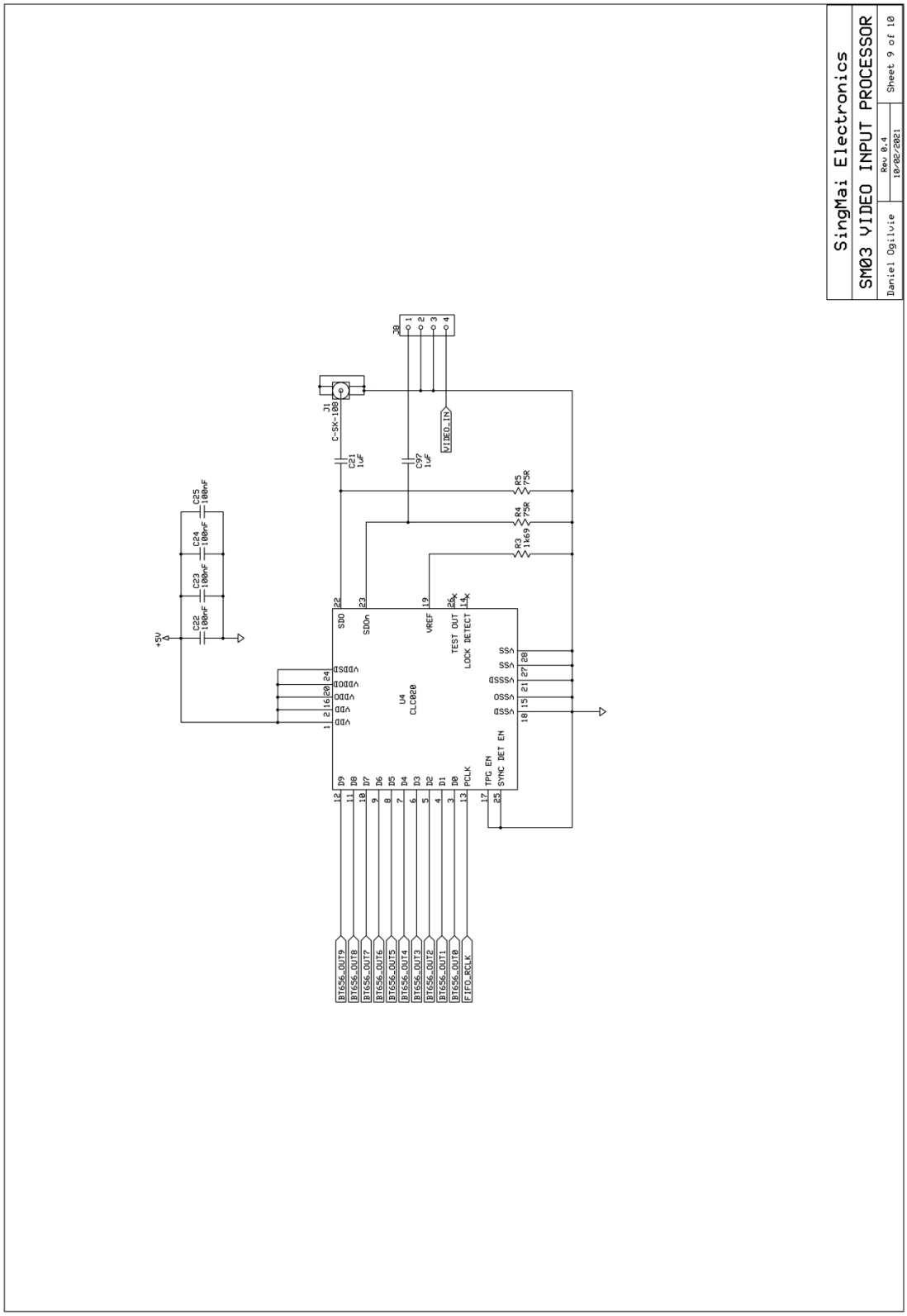

Figure 24 SM03 schematics- Sheet 9.

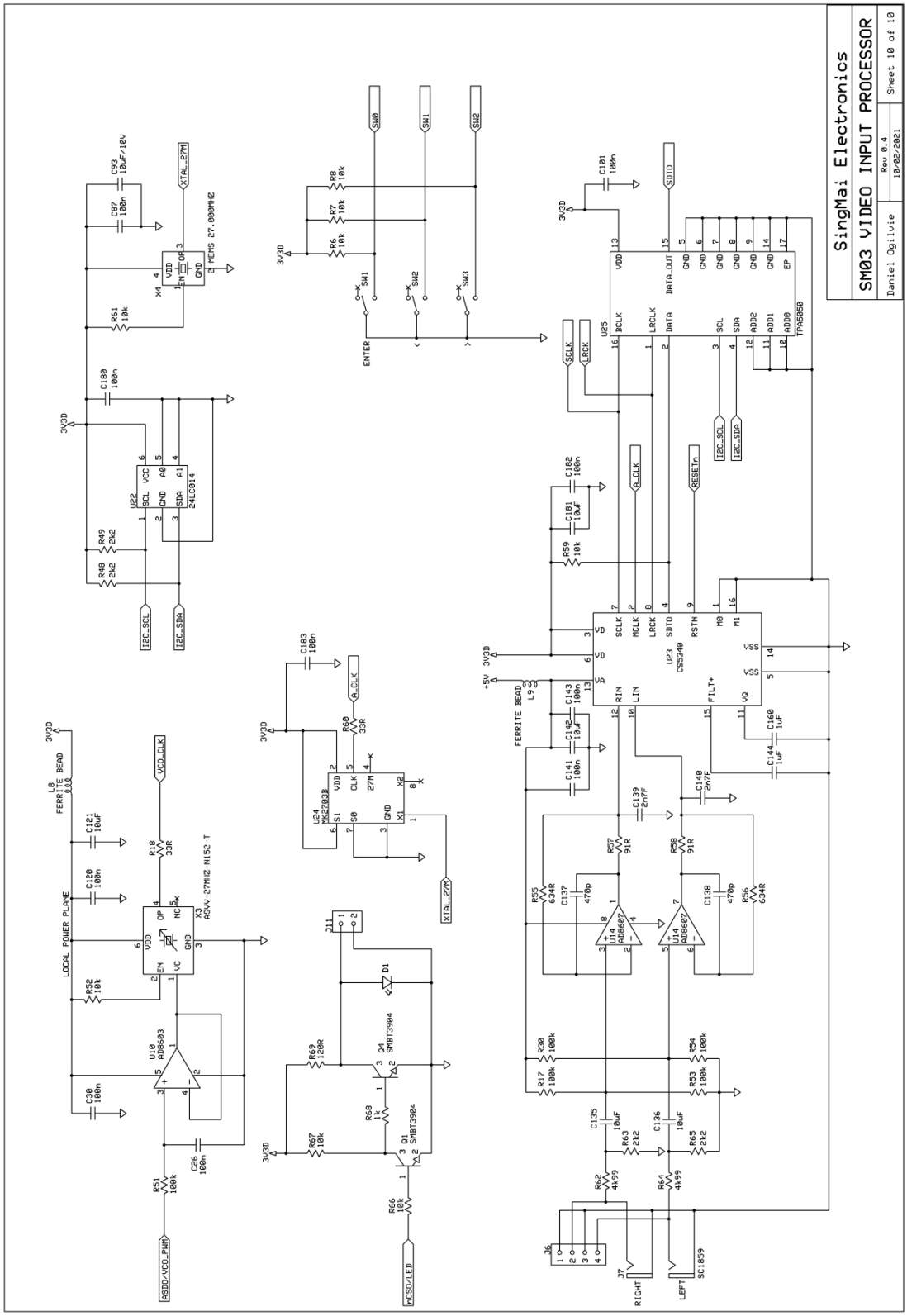

Figure 25 SM03 schematics- Sheet 10.

7. Re-programming the FPGA

The FPGA may be reprogrammed to install new features or improvements. As the SM03 uses an Altera FPGA it is necessary to download the Quartus programmer software (free from the Altera website: https://wl.altera.com/download/software/prog-software/12.1). It may be necessary to register on their website, but the software is free. Please ensure that you only download version 12.1 as the later versions of the software do not support the FPGA used by the SM03.

Also it is necessary to use the USB-Blaster module, also from Altera (or similar from other companies): http://www.buyaltera.com/scripts/partsearch.dll?Detail&name=544-1775-ND.

The USB-Blaster 10-way header plugs into J4, the 10W header on the SM03. The header is polarized to ensure the cable cannot be inserted the wrong way (see Figures 26 and 27).

Figure 26 Re-programming the SM03.

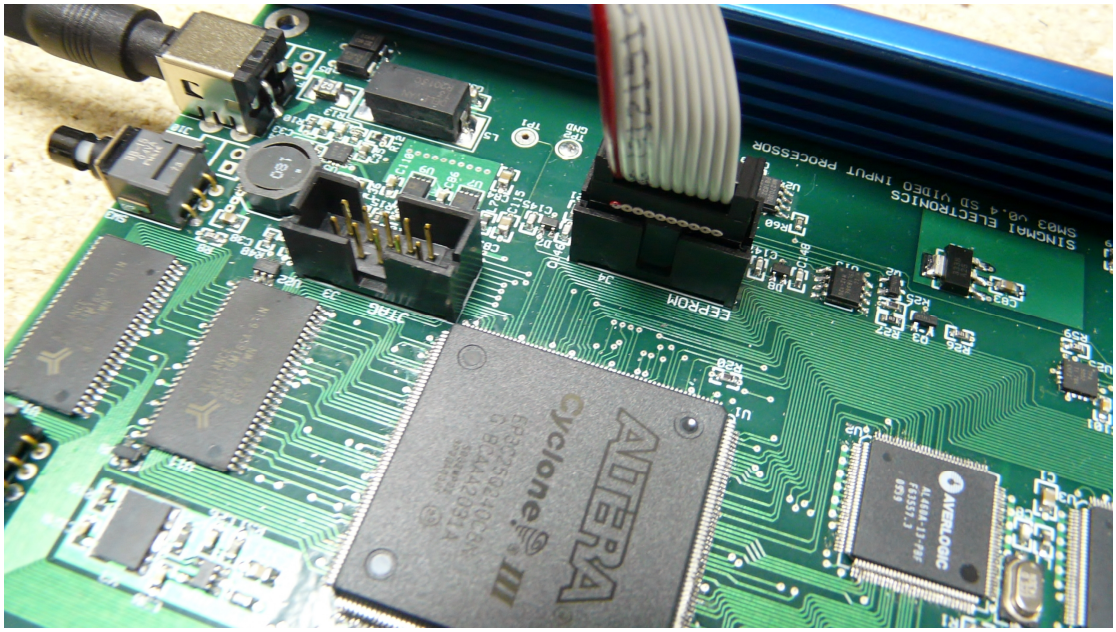

Figure 27 Re-programming the SM03 - detail.

Install and open the Quartus programmer. The screen should look similar to Figure 28. Ensure the SM03 is powered on.

The new FPGA image will be sent as a file called SB03.pof. Set the programming mode to 'Active Serial Programming'. If everything is OK the programmer should recognize the serial EEPROM (shown as EPCS16). Click the 'Add File' button and point to the SM03.pof file. Click the check box 'Program/Configure' and click the 'Start' button. You should see the progress bar move as the device is programmed. If successful the bar will show 100% (Successful) after programming is complete and 'FPGA OK' LED should light (see Figure .

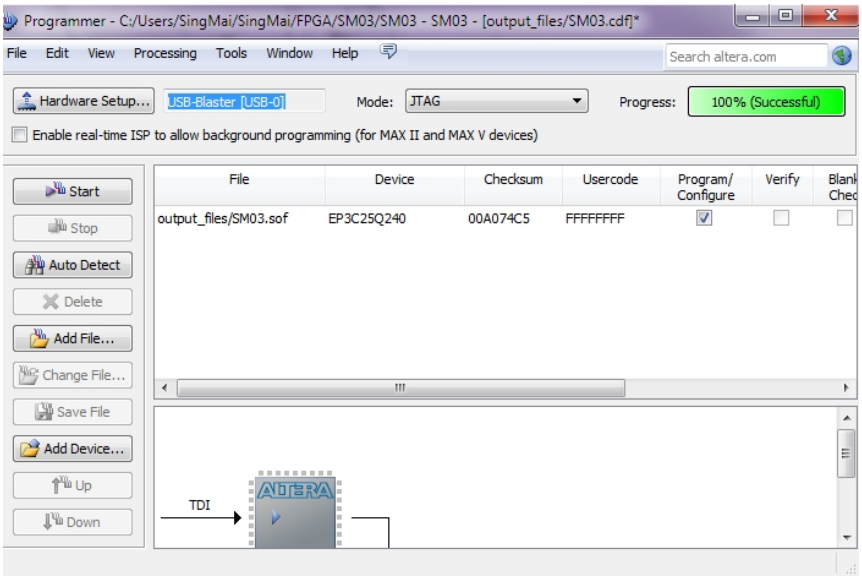

Figure 28 Quartus FPGA programmer.

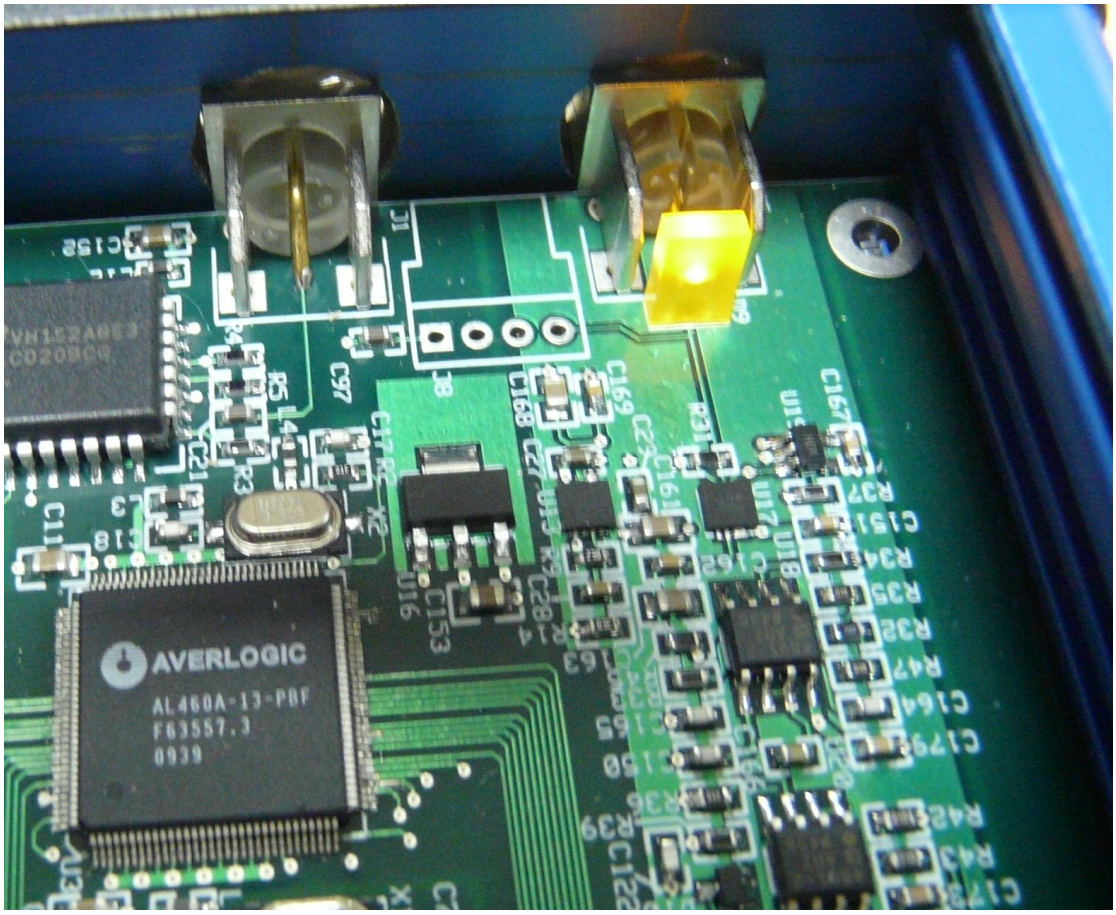

Figure 29 FPGA program OK LED.

8. Specification

Power:	+5VDC ± 5% @ ~650mA.
Dimensions:	160mm x 78mm x 27mm.
CVBS input:	NTSC-M / PAL / SECAM (auto detected). 75Ω input impedance.
Luma bandwidth:	5.5MHz ± 0.2dB.
Chroma bandwidth:	1.3MHz - 3dB.
Differential gain/phase:	<1%, <1°.
K-factor:	<1%.
Luma/chroma delay:	< ±10ns.
Signal to noise ratio:	< -55dB unified weighting (Y channel, noise reduction off).
Output:	SDI format (SMPTE-259M).
Latency:	<1 frames (40ms maximum) + 100µs (1 frame latency caused by synchronizer).
Operating temperature:	0 – 40 degC.

Appendix A: AC-DC adaptor

The specification for the supplied AC-DC adaptor (TE10A0503F01) is shown in Figures 30-32.

TE10 Family

10W–12W Single Output External Power
Industrial Grade

FEATURES AND BENEFITS

Universal Input 90VAC–264VAC Input Range Desktop and Wall-Plug Versions	Meets "Heavy Industrial" Levels of EN61000 EMC Requirements
Up to 12W of AC-DC Power	>10 Year E-Cap Life
IP22 Rated Enclosure	>1,000,000 Hours MTBF
Approved to EN/IEC/UL60950-1 2nd Edition, Am.2	3 Year Warranty
Meets EN55022/CISPR22, FCC Part 15.109 Class B Conducted & Radiated Emissions, with 6db Margin	Meets DoE Efficiency Level VI Requirements No Load Input Power Average Efficiency

MODEL SELECTION

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503F01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class I Desktop, IEC60320 C14 Receptacle
TE10A0603F01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703F01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203F01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403F01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503N01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C8 Receptacle
TE10A0603N01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703N01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203N01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403N01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503Q01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C18 Receptacle
TE10A0603Q01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703Q01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203Q01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403Q01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503B01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Interchangeable Blades (North American Blade included)[2]
TE10A0603B01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703B01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203B01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403B01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

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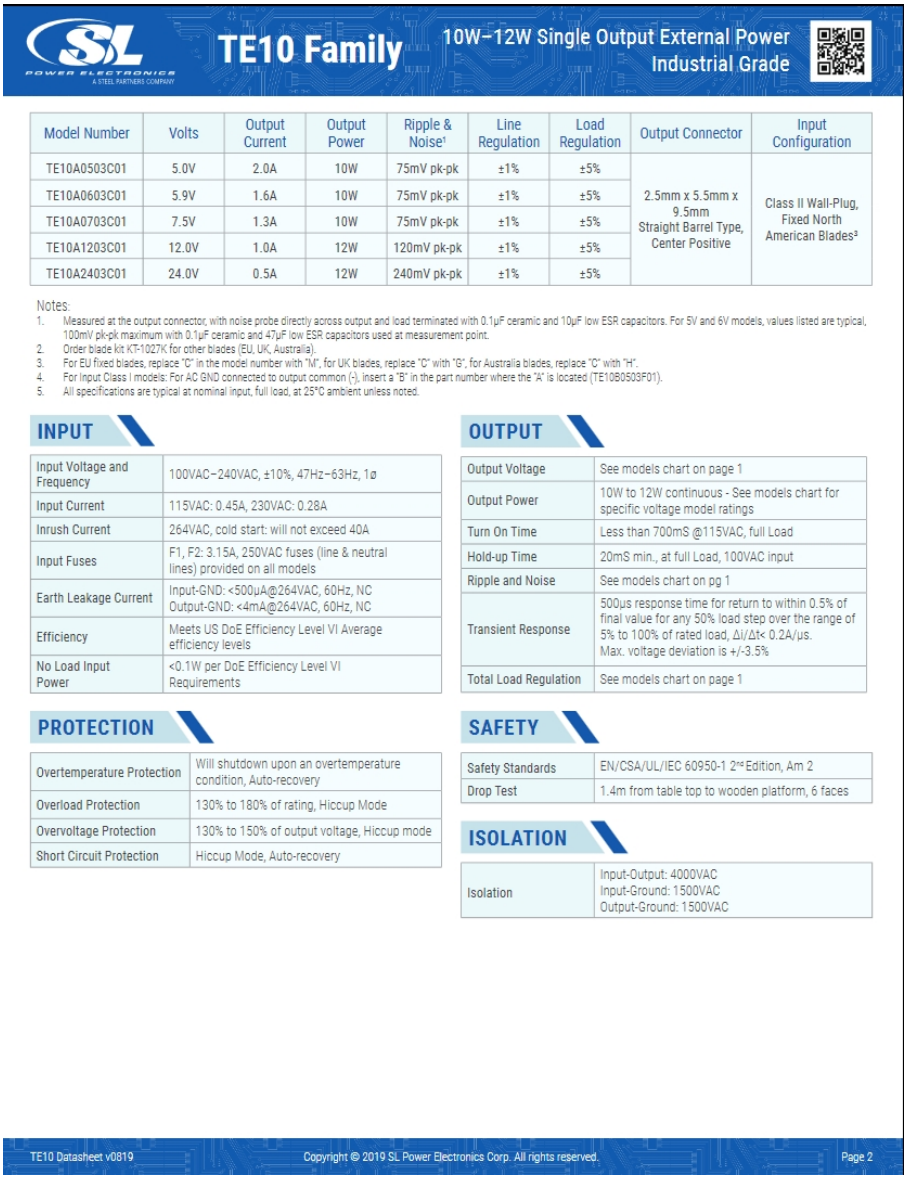
Figure 30 Power supply specification – Page 1.



SL POWER ELECTRONICS
A STEEL PARTNERS COMPANY

TE10 Family

10W–12W Single Output External Power
Industrial Grade

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503C01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Fixed North American Blades[2]
TE10A0603C01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703C01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203C01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403C01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

Notes:
1. Measured at the output connector, with noise probe directly across output and load terminated with 0.1µF ceramic and 10µF low ESR capacitors. For 5V and 6V models, values listed are typical, 100mV pk-pk maximum with 0.1µF ceramic and 47µF low ESR capacitors used at measurement point.
2. Order blade kit KT-1027K for other blades (EU, UK, Australia).
3. For EU fixed blades, replace "C" in the model number with "M", for UK blades, replace "C" with "G", for Australia blades, replace "C" with "H".
4. For Input Class I models: For AC GND connected to output common (-), insert a "B" in the part number where the "A" is located (TE10B0503F01).
5. All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

INPUT

Input Voltage and Frequency	100VAC–240VAC, ±10%, 47Hz–63Hz, 1ø
Input Current	115VAC: 0.45A, 230VAC: 0.28A
Inrush Current	264VAC, cold start: will not exceed 40A
Input Fuses	F1, F2: 3.15A, 250VAC fuses (line & neutral lines) provided on all models
Earth Leakage Current	Input-GND: <500µA@264VAC, 60Hz, NC Output-GND: <4mA@264VAC, 60Hz, NC
Efficiency	Meets US DoE Efficiency Level VI Average efficiency levels
No Load Input Power	<0.1W per DoE Efficiency Level VI Requirements

OUTPUT

Output Voltage	See models chart on page 1
Output Power	10W to 12W continuous - See models chart for specific voltage model ratings
Turn On Time	Less than 700mS @115VAC, full Load
Hold-up Time	20mS min., at full Load, 100VAC input
Ripple and Noise	See models chart on pg 1
Transient Response	500µs response time for return to within 0.5% of final value for any 50% load step over the range of 5% to 100% of rated load, Δi/Δt< 0.2A/µs. Max. voltage deviation is +/-3.5%
Total Load Regulation	See models chart on page 1

PROTECTION

Overtemperature Protection	Will shutdown upon an overtemperature condition, Auto-recovery
Overload Protection	130% to 180% of rating, Hiccup Mode
Overvoltage Protection	130% to 150% of output voltage, Hiccup mode
Short Circuit Protection	Hiccup Mode, Auto-recovery

SAFETY

Safety Standards	EN/CSA/UL/IEC 60950-1 2nd Edition, Am 2
Drop Test	1.4m from table top to wooden platform, 6 faces

ISOLATION

Isolation	Input-Output: 4000VAC Input-Ground: 1500VAC Output-Ground: 1500VAC

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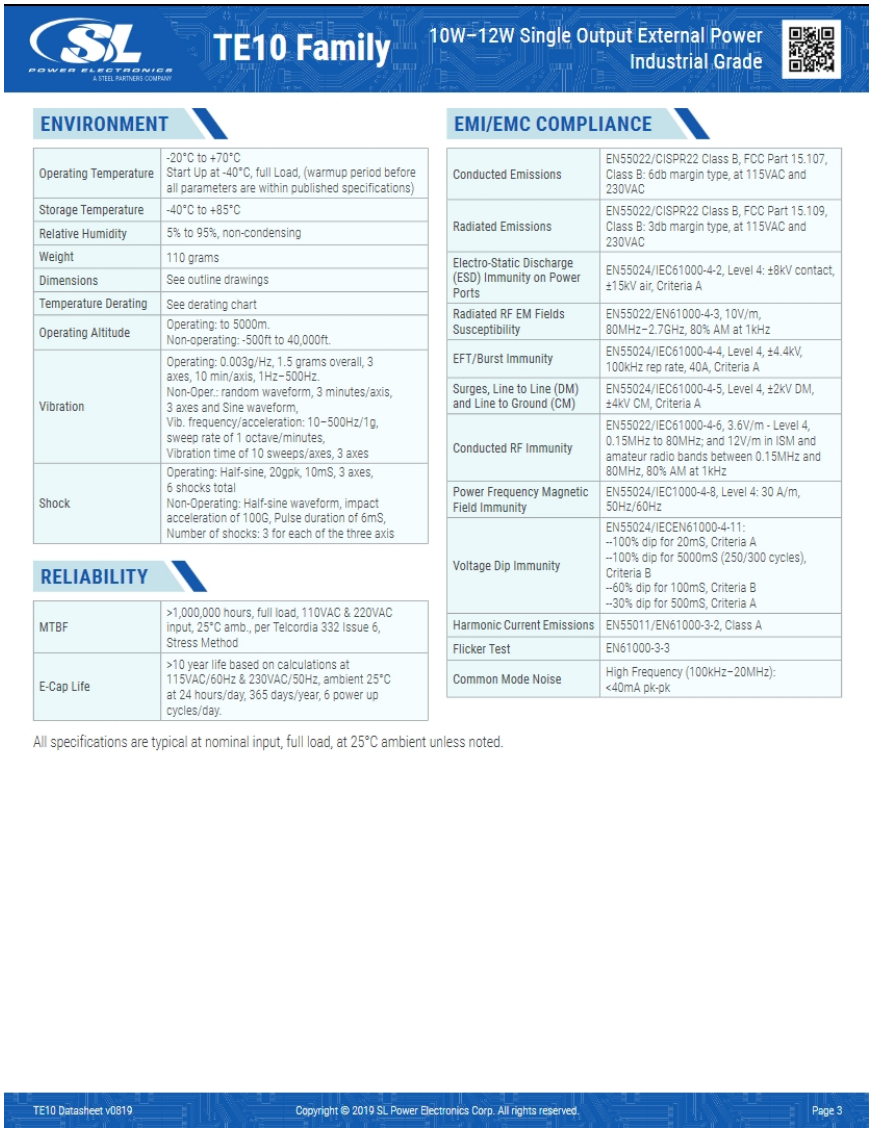
Figure 31 Power supply specification – Page 2.



TE10 Family

10W–12W Single Output External Power
Industrial Grade

ENVIRONMENT

Operating Temperature	-20°C to +70°C Start Up at -40°C, full Load, (warmup period before all parameters are within published specifications)
Storage Temperature	-40°C to +85°C
Relative Humidity	5% to 95%, non-condensing
Weight	110 grams
Dimensions	See outline drawings
Temperature Derating	See derating chart
Operating Altitude	Operating: to 5000m. Non-operating: -500ft to 40,000ft.
Vibration	Operating: 0.003g/Hz, 1.5 grams overall, 3 axes, 10 min/axis, 1Hz–500Hz. Non-Oper.: random waveform, 3 minutes/axis, 3 axes and Sine waveform, Vib. frequency/acceleration: 10–500Hz/1g, sweep rate of 1 octave/minutes, Vibration time of 10 sweeps/axes, 3 axes
Shock	Operating: Half-sine, 20gpk, 10mS, 3 axes, 6 shocks total Non-Operating: Half-sine waveform, impact acceleration of 100G, Pulse duration of 6mS, Number of shocks: 3 for each of the three axis

RELIABILITY

MTBF	>1,000,000 hours, full load, 110VAC & 220VAC input, 25°C amb., per Telcordia 332 Issue 6, Stress Method
E-Cap Life	>10 year life based on calculations at 115VAC/60Hz & 230VAC/50Hz, ambient 25°C at 24 hours/day, 365 days/year, 6 power up cycles/day.

EMI/EMC COMPLIANCE

Conducted Emissions	EN55022/CISPR22 Class B, FCC Part 15.107, Class B: 6db margin type, at 115VAC and 230VAC
Radiated Emissions	EN55022/CISPR22 Class B, FCC Part 15.109, Class B: 3db margin type, at 115VAC and 230VAC
Electro-Static Discharge (ESD) Immunity on Power Ports	EN55024/IEC61000-4-2, Level 4: ±8kV contact, ±15kV air, Criteria A
Radiated RF EM Fields Susceptibility	EN55022/EN61000-4-3, 10V/m, 80MHz–2.7GHz, 80% AM at 1kHz
EFT/Burst Immunity	EN55024/IEC61000-4-4, Level 4, ±4.4kV, 100kHz rep rate, 40A, Criteria A
Surges, Line to Line (DM) and Line to Ground (CM)	EN55024/IEC61000-4-5, Level 4, ±2kV DM, ±4kV CM, Criteria A
Conducted RF Immunity	EN55022/IEC61000-4-6, 3.6V/m - Level 4, 0.15MHz to 80MHz; and 12V/m in ISM and amateur radio bands between 0.15MHz and 80MHz, 80% AM at 1kHz
Power Frequency Magnetic Field Immunity	EN55024/IEC1000-4-8, Level 4: 30 A/m, 50Hz/60Hz
Voltage Dip Immunity	EN55024/IECEN61000-4-11: –100% dip for 20mS, Criteria A –100% dip for 5000mS (250/300 cycles), Criteria B –60% dip for 100mS, Criteria B –30% dip for 500mS, Criteria A
Harmonic Current Emissions	EN55011/EN61000-3-2, Class A
Flicker Test	EN61000-3-3
Common Mode Noise	High Frequency (100kHz–20MHz): <40mA pk-pk

All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

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Figure 32 Power supply specification – Page 3.