SM06

Advanced Composite Video Interface:

aCVi Transmitter module

User Manual

Revision 0.1
22nd February 2020

Revision History

Date	Revisions	Version
20-02-2020	First Draft.	0.1

Contents

Figures

1. Introduction

aCVi® is a proprietary interface for transmitting high definition video over long distances of coaxial or twisted-pair cable.

SM06 is a transmitter module compatible with the aCVi® Advanced Composite Video Interface format. SM06 accepts DVI or HD-SDI input formats which it converts to analogue aCVi® encoded video for driving long distances of both twisted pair and low cost coaxial cable.

SM06 supports the following HD standards: 720p-25/30/50/59.94/60Hz and 1080p-24/25/29.97/30Hz. Switching between standards is automatic.

Figure 1 SM06 module.

The compatible aCVi® receiver for the SM06 transmitter is the SM08 (HD-SDI output).

Other aCVi® modules/boards include:

PT56 aCVi encoder IP core.

PT52 aCVi decoder IP core.

SM02 aCVi video test pattern generator.

For the latest list of available modules follow this link.

2. aCVi Overview

The following is a brief overview of the aCVi® revision 2 interface (abbreviated to aCVi® in this document).

aCVi® is a proprietary format, developed by SingMai Electronics, to transmit high definition video over long distances of coaxial or twisted pair cable. aCVi® is an update to the previous version, specifically designed to interface directly to image sensors, although it may also be used to transmit conventional video sources.

A single chip image sensor, as found in almost all non-broadcast cameras, uses a colour filter to 'assign' each sensor pixel one of red, green or blue sensitivities. Because green is where the human eye is most sensitive, there are twice as many green pixels as red and blue (see Figure 2). This means that if your sensor has a horizontal array of 1920 pixels, only 960 of them are green, red or blue pixels, and for the red and blue pixels, each horizontal line is either red or blue. The actual resolution of the sensor to each colour is for green, 960 x 1080 pixels, and for red and blue, 960 x 540 pixels. (A broadcast camera will use three optically aligned sensors, each offering 1920 x 1080 pixels for the three colours). If we refer to the full resolution (e.g. a broadcast camera) as 4:4:4 sampled, a single image sensor actually produces a 2:2:0 output.

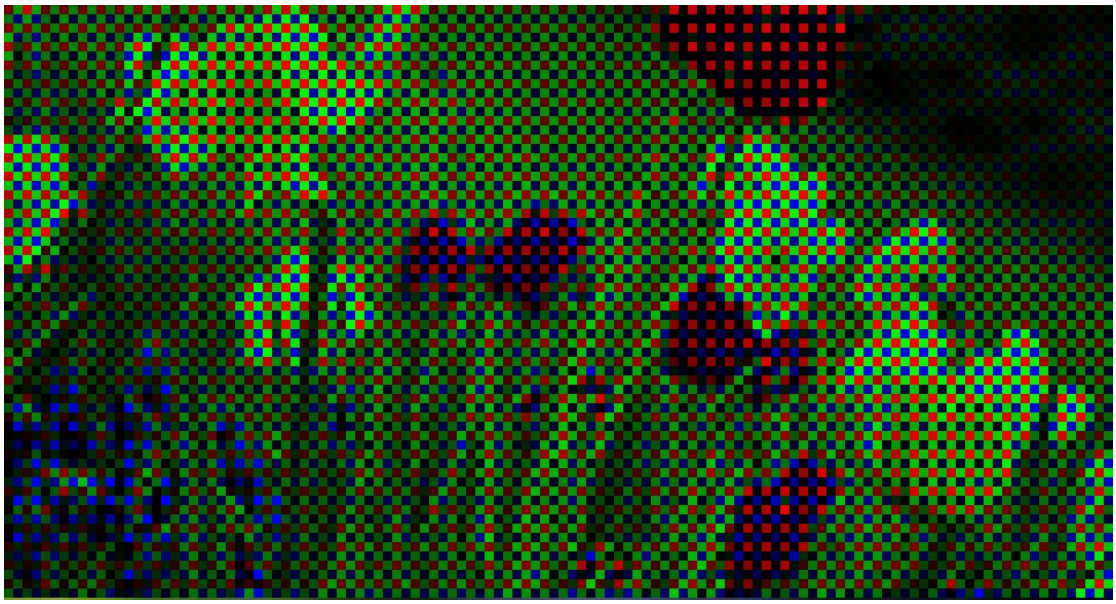


Figure 2 Bayer colour filter.

To conform with video standards (e.g. 1920 x 1080) the additional pixels are interpolated (a technique known as Bayer de-mosaicing) and this function is usually performed in the camera ISP (Image Signal Processor). However this process can produce artifacts into the image (for example see the colour artifacts on the white fence in Figure 3), and also, because it generates more than double the amount of original pixels, more than doubles the bandwidth of the output signal, which exacerbates the problem if the video is required to transmitted long distances.

aCVi® interfaces directly to the single chip image sensor and transmits the RAW 2:2:0 resolution image directly, thereby reducing by more than half the bandwidth of the transmitted signal and achieving higher resolution, lower noise and greater distances.

Figure 3 Left: Original full resolution image. Right: Image after Bayer demosaicing.

The available aCVi® modules are shown in Figure 4. The SM06 provides an aCVi® transmitter for HD-SDI or DVI video sources (e.g. a video camera) and simultaneously drives both coaxial and twisted-pair cable.

The receiver module is the SM08. This module accepts either twisted-pair or coaxial cable and converts the aCVi® video to an HD-SDI output for a TV monitor or video recorder.

Figure 4 aCVi® Modules.

3. Connecting up the module

The SM06 module is powered by a universal input (90-260VAC) AC-DC adaptor (see Appendix A for the power supply specification). The 5VDC, 12W output of this adaptor should be connected to the jack input, '+5V IN', of the SM06. Once connected, the yellow LED, 'FPGA OK' should light, indicating the FPGA has been correctly configured and the module is running.

Figure 5 shows the interconnections for SM06.

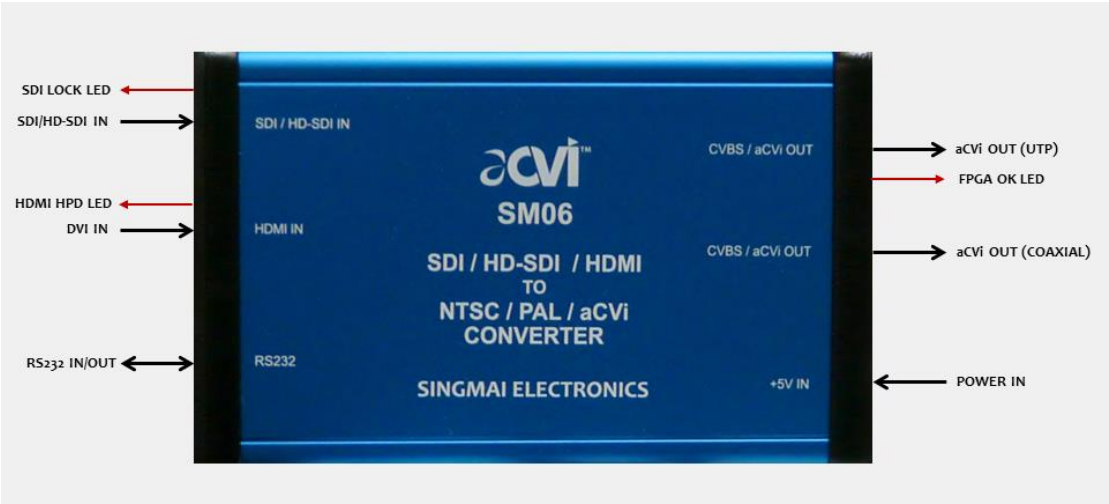


Figure 5 SM06 Interconnections.

SM06 accepts HD-SDI or DVI inputs: priority is given to the HD-SDI input if both inputs are connected simultaneously.

Switching between the input standards is automatic. If a valid HD-SDI clock is detected on the input, the 'SDI LOCK' LED will light. If the HD-SDI input has valid TRS timing pulses and is one of the supported aCVi® video standards (720p-25/30/50/59.94/60Hz and 1080p-24/25/29.97/30Hz) the aCVi® encoder will convert the HD-SDI signal to an aCVi® output.

If a valid DVI input is connected and the HD-SDI input is not connected, the HDMI HPD LED will light (Hot Plug Detect) the aCVi® encoder will convert the DVI signal to an aCVi® output.

SM06 provides simultaneous single ended coaxial and differential twisted-pair (UTP) outputs. The UTP outputs are connected via a RJ45 style connector. Figure 7 shows the pin assignments for the connector: aCVi® assumes the UTP cable connections are 'straight' so both the transmitter and receiver use pin 1 for the 'VIDEO+' (non-inverted) signal, and pin 2 'VIDEO-' (inverted) signal.

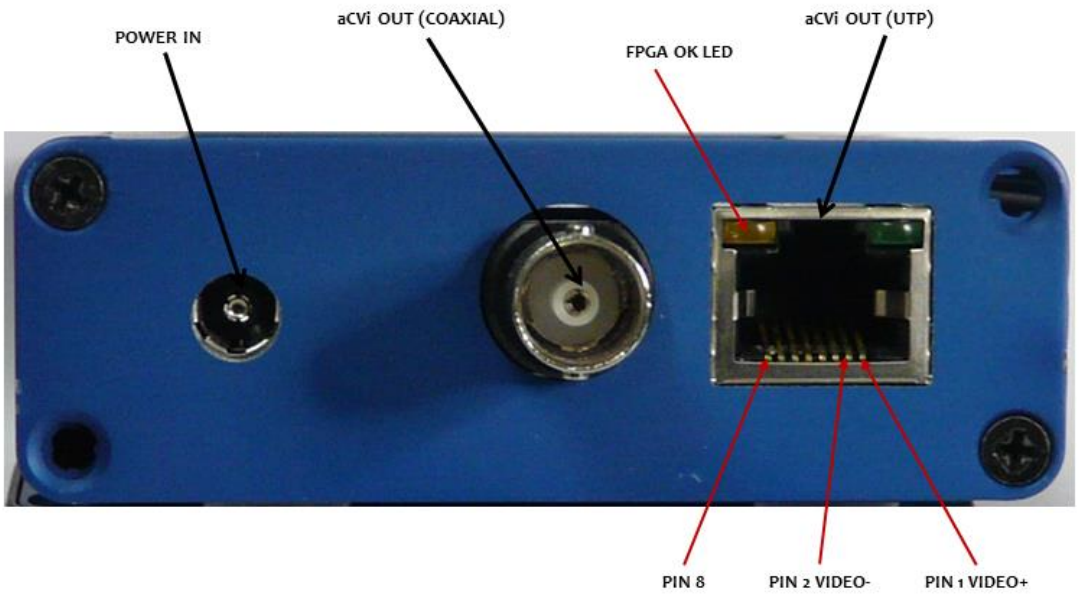


Figure 6 UTP connector pin assignments.

Should the inputs to the SM06 be removed or fail, the SM06 will switch to an internal colour bar generator. The output video standard will be whatever was last detected on the inputs (e.g. if the last detected input was 1080p/30Hz, the output will be 75% colour bars at 1080p/30Hz standard). If no valid input has previously been detected, the colour bar output will default to 720p/60Hz. Note that the colour bar generator will default to 720p/60Hz if the last input standard was either 720p/59.94Hz, 1080p/29.97Hz or 1080i/59.94Hz.

4. Circuit description

Figures 14-23 show the schematics for the SM06. Below is a brief technical description of the module.

Sheet 1.
J3 is the 5VDC power input connector to the SM06 module. The 5VDC is protected from reverse polarity and over-range inputs by D1, D2 and the resettable fuse, F1. The input is then filtered by L1 and C2 to provide the 'clean' 5VDC for the analogue output stage and also linearly regulated by U1 and U20 to provide the 3.3VDC and 2.5VDC supply voltages.

Sheet 2.
U2 provides the 1.2VDC for the internal voltage of the FPGA. U3 provides the 2.5VDC for the analogue PLL circuity of the FPGA and L2 and C25 filter the VCCINT for the FPGA PLL digital blocks. U12 provides the 1.8V for the HDMI receiver with LC networks providing isolation for the various individual rails.

Sheet 3.
J1 is the DVI/HDMI input connector. U13 and U14 protect the HDMI receiver from overshoots on the TMDS signals and U15 does the same for the control signals. The hot plug detect signal, indicating the presence of a HDMI source, is shown by LED, D5.

Sheet 4.
U16 is the HDMI receiver IC, an Analog Devices ADV7611. The output from this IC is Y,Cb,Cr in 4:2:2 format. In free-run mode this IC provides the fixed 74.25MHz clock. The video input standard is read from the ADV7611 status registers.

Sheet 5.
U4 is the cable equalizer for the HD-SDI input. U18 deserialises the 1.485GHz input to five LVDS inputs and a DDR clock. Further demuxing, extraction of the TRS timing signals and the video formatting is performed by the FPGA. LED D9 lights if U18 is able to lock to incoming HD-SDI signal. The input standard is also determined by the FPGA.

Sheet 6.
U19 is the FPGA. The FPGA is an Altera EP4CE15 device in a 144 pin 0.5mm TQFP package. The FPGA contains the PT56 aCVi® encoder, a SingMai PT13 control microprocessor, a colour bar generator and the HD-SDI input decoder.

Sheet 7.
The FPGA is a volatile device and needs configuring on switch on, which it does using U5, a 4Mb EEPROM. The device is automatically configured on switch on, and successful configuration is indicated by LED, 'FPGA OK'. The EEPROM may also be reprogrammed via J4, which is compatible with the Altera 'USB-Blaster' and the Quartus Programmer.

Sheet 8.
X1 is a 27MHz crystal oscillator, and is used to clock the PT13 microprocessor and also as a fixed time-base to determine the HD-SDI input standard.

U7 is a proprietary copy-protection IC. U7 calculates a checksum from a PT13 generated data stream, and the calculated checksum from U7 is compared with an FPGA internally generated checksum. If the two do not match the SM06 module is shut down. This means that even if the bit stream of the FPGA/EEPROM is captured the PT56 IP core will not run without U7 being fitted.

U17 is an RS232 level translator used for the data interface.

Sheet 9.

U8 is a 10 bit digital to analogue converter (DAC). The DAC converts the aCVi® encoded digital data to an analogue signal of 0 - 1.0V amplitude. The DAC is clocked at 148.5MHz. U6 provides a 'clean' 3.3V for the DAC. U21 amplifies the DAC output to provide a 1.8V pk-pk output for driving the outputs and U9 provides a programmable low pass filter to remove the clock from output video and reconstitute the waveform.

Sheet 10.

U10-A buffers the coaxial aCVi® video and U10-B filters the input signal. C50 and Q6 form a black level clamp to remove the sync pulse and ensure stable DC levels into the data slicer. The data slicer is formed by comparator U10-D and buffered by U11 before being decoded by the PT56 aCVi® encoder IP core.

5. Specification

Power:	+5VDC ± 5% @ ~450mA.
Dimensions:	120mm x 78mm x 27mm.
HD-SDI input:	SMPTE-292M, 20 bit 4:2:2 YCbCr format.
Video standards:	720p/25Hz,720p/30Hz, 720p/50Hz, 720p/59.94Hz, 720p/60Hz 1080p/25Hz, 1080p/29.97Hz, 1080p/30Hz.
Luma bandwidth:	14MHz ± 1dB. >-50dB @ 17.6MHz.
Chroma bandwidth:	14MHz ± 1dB. >-40dB @ 17.6MHz.
Transmission distance:	>300m of RG-59 coaxial cable. >500m RG-59 cable with reduced luma bandwidth.
Latency:	<100µs (transmitter HD-SDI input to receiver HD-SDI output).
Operating temperature:	-10° to +45°degC.

Appendix A: Power supply specification

The AC-DC converter supplied with the SM06 is a model TE10A0503F01 from SL Power Electronics. It accepts all AC inputs from 90-264VAC and provides a 5V, 2A DC output for the SM06. The detailed specification is shown below.

TE10 Family 10W~12W Single Output External Power Industrial Grade

FEATURES AND BENEFITS

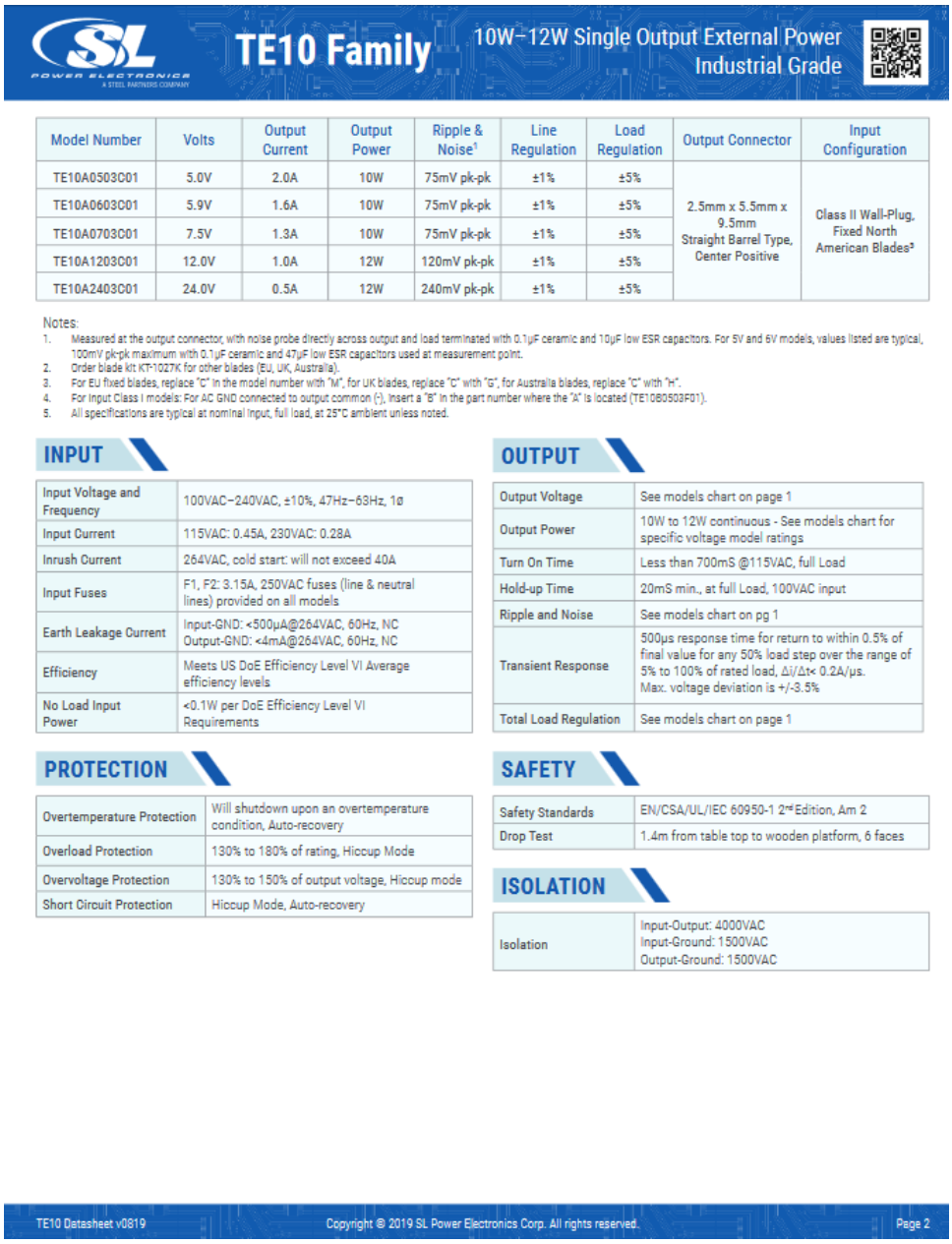
Universal Input 90VAC~264VAC Input Range Desktop and Wall-Plug Versions	Meets "Heavy Industrial" Levels of EN61000 EMC Requirements
Up to 12W of AC-DC Power	>10 Year E-Cap Life
IP22 Rated Enclosure	>1,000,000 Hours MTBF
Approved to EN/IEC/UL60950-1 2nd Edition, Am.2	3 Year Warranty
Meets EN55022/CISPR22, FCC Part 15.109 Class B Conducted & Radiated Emissions, with 6db Margin	Meets DoE Efficiency Level VI Requirements No Load Input Power Average Efficiency

MODEL SELECTION

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503F01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class I Desktop, IEC60320 C14 Receptacle
TE10A0603F01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703F01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203F01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403F01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503N01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C8 Receptacle
TE10A0603N01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703N01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203N01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403N01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503Q01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C18 Receptacle
TE10A0603Q01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703Q01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203Q01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403Q01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503B01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Interchangeable Blades (North American Blade included)[2]
TE10A0603B01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703B01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203B01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403B01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

TE10 Datasheet v0819 Page 1

Figure 7 Power supply specification - page 1.



SL POWER ELECTRONICS — A STEEL PARTNERS COMPANY

TE10 Family

10W–12W Single Output External Power
Industrial Grade

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503C01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Fixed North American Blades[3]
TE10A0603C01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703C01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203C01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403C01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

Notes:
1. Measured at the output connector, with noise probe directly across output and load terminated with 0.1µF ceramic and 10µF low ESR capacitors. For 5V and 6V models, values listed are typical, 100mV pk-pk maximum with 0.1µF ceramic and 47µF low ESR capacitors used at measurement point.
2. Order blade kit KT-1027K for other blades (EU, UK, Australia).
3. For EU fixed blades, replace "C" in the model number with "M", for UK blades, replace "C" with "G", for Australia blades, replace "C" with "H".
4. For Input Class I models: For AC GND connected to output common (-), insert a "B" in the part number where the "A" is located (TE10B0503F01).
5. All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

INPUT

Input Voltage and Frequency	100VAC–240VAC, ±10%, 47Hz–63Hz, 1ø
Input Current	115VAC: 0.45A, 230VAC: 0.28A
Inrush Current	264VAC, cold start: will not exceed 40A
Input Fuses	F1, F2: 3.15A, 250VAC fuses (line & neutral lines) provided on all models
Earth Leakage Current	Input-GND: <500µA@264VAC, 60Hz, NC Output-GND: <4mA@264VAC, 60Hz, NC
Efficiency	Meets US DoE Efficiency Level VI Average efficiency levels
No Load Input Power	<0.1W per DoE Efficiency Level VI Requirements

OUTPUT

Output Voltage	See models chart on page 1
Output Power	10W to 12W continuous - See models chart for specific voltage model ratings
Turn On Time	Less than 700mS @115VAC, full Load
Hold-up Time	20mS min., at full Load, 100VAC input
Ripple and Noise	See models chart on pg 1
Transient Response	500µs response time for return to within 0.5% of final value for any 50% load step over the range of 5% to 100% of rated load, Δi/Δt< 0.2A/µs. Max. voltage deviation is +/-3.5%
Total Load Regulation	See models chart on page 1

PROTECTION

Overtemperature Protection	Will shutdown upon an overtemperature condition, Auto-recovery
Overload Protection	130% to 180% of rating, Hiccup Mode
Overvoltage Protection	130% to 150% of output voltage, Hiccup mode
Short Circuit Protection	Hiccup Mode, Auto-recovery

SAFETY

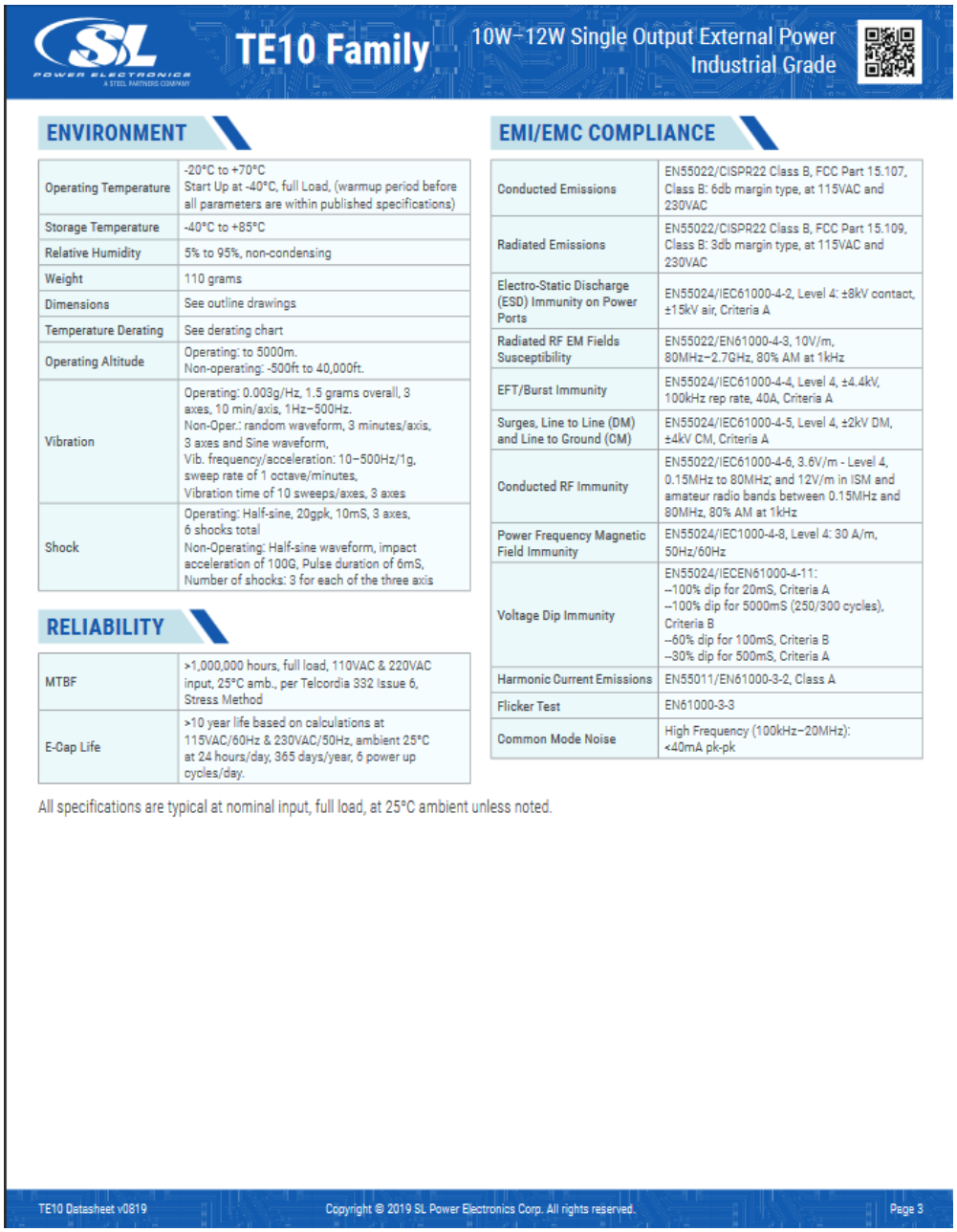
Safety Standards	EN/CSA/UL/IEC 60950-1 2nd Edition, Am 2
Drop Test	1.4m from table top to wooden platform, 6 faces

ISOLATION

Isolation	Input-Output: 4000VAC Input-Ground: 1500VAC Output-Ground: 1500VAC

TE10 Datasheet v0819 Page 2

Figure 8 Power supply specification - page 2.



TE10 Family

10W–12W Single Output External Power
Industrial Grade

ENVIRONMENT

Operating Temperature	-20°C to +70°C Start Up at -40°C, full Load, (warmup period before all parameters are within published specifications)
Storage Temperature	-40°C to +85°C
Relative Humidity	5% to 95%, non-condensing
Weight	110 grams
Dimensions	See outline drawings
Temperature Derating	See derating chart
Operating Altitude	Operating: to 5000m. Non-operating: -500ft to 40,000ft.
Vibration	Operating: 0.003g/Hz, 1.5 grams overall, 3 axes, 10 min/axis, 1Hz–500Hz. Non-Oper.: random waveform, 3 minutes/axis, 3 axes and Sine waveform, Vib. frequency/acceleration: 10–500Hz/1g, sweep rate of 1 octave/minutes, Vibration time of 10 sweeps/axes, 3 axes
Shock	Operating: Half-sine, 20gpk, 10mS, 3 axes, 6 shocks total Non-Operating: Half-sine waveform, impact acceleration of 100G, Pulse duration of 6mS, Number of shocks: 3 for each of the three axis

RELIABILITY

MTBF	>1,000,000 hours, full load, 110VAC & 220VAC input, 25°C amb., per Telcordia 332 Issue 6, Stress Method
E-Cap Life	>10 year life based on calculations at 115VAC/60Hz & 230VAC/50Hz, ambient 25°C at 24 hours/day, 365 days/year, 6 power up cycles/day.

EMI/EMC COMPLIANCE

Conducted Emissions	EN55022/CISPR22 Class B, FCC Part 15.107, Class B: 6db margin type, at 115VAC and 230VAC
Radiated Emissions	EN55022/CISPR22 Class B, FCC Part 15.109, Class B: 3db margin type, at 115VAC and 230VAC
Electro-Static Discharge (ESD) Immunity on Power Ports	EN55024/IEC61000-4-2, Level 4: ±8kV contact, ±15kV air, Criteria A
Radiated RF EM Fields Susceptibility	EN55022/EN61000-4-3, 10V/m, 80MHz–2.7GHz, 80% AM at 1kHz
EFT/Burst Immunity	EN55024/IEC61000-4-4, Level 4, ±4.4kV, 100kHz rep rate, 40A, Criteria A
Surges, Line to Line (DM) and Line to Ground (CM)	EN55024/IEC61000-4-5, Level 4, ±2kV DM, ±4kV CM, Criteria A
Conducted RF Immunity	EN55022/IEC61000-4-6, 3.6V/m - Level 4, 0.15MHz to 80MHz; and 12V/m in ISM and amateur radio bands between 0.15MHz and 80MHz, 80% AM at 1kHz
Power Frequency Magnetic Field Immunity	EN55024/IEC1000-4-8, Level 4: 30 A/m, 50Hz/60Hz
Voltage Dip Immunity	EN55024/IECEN61000-4-11: –100% dip for 20mS, Criteria A –100% dip for 5000mS (250/300 cycles), Criteria B –60% dip for 100mS, Criteria B –30% dip for 500mS, Criteria A
Harmonic Current Emissions	EN55011/EN61000-3-2, Class A
Flicker Test	EN61000-3-3
Common Mode Noise	High Frequency (100kHz–20MHz): <40mA pk-pk

All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

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Figure 9 Power supply specification - page 3.

Appendix B: SM06 Schematics

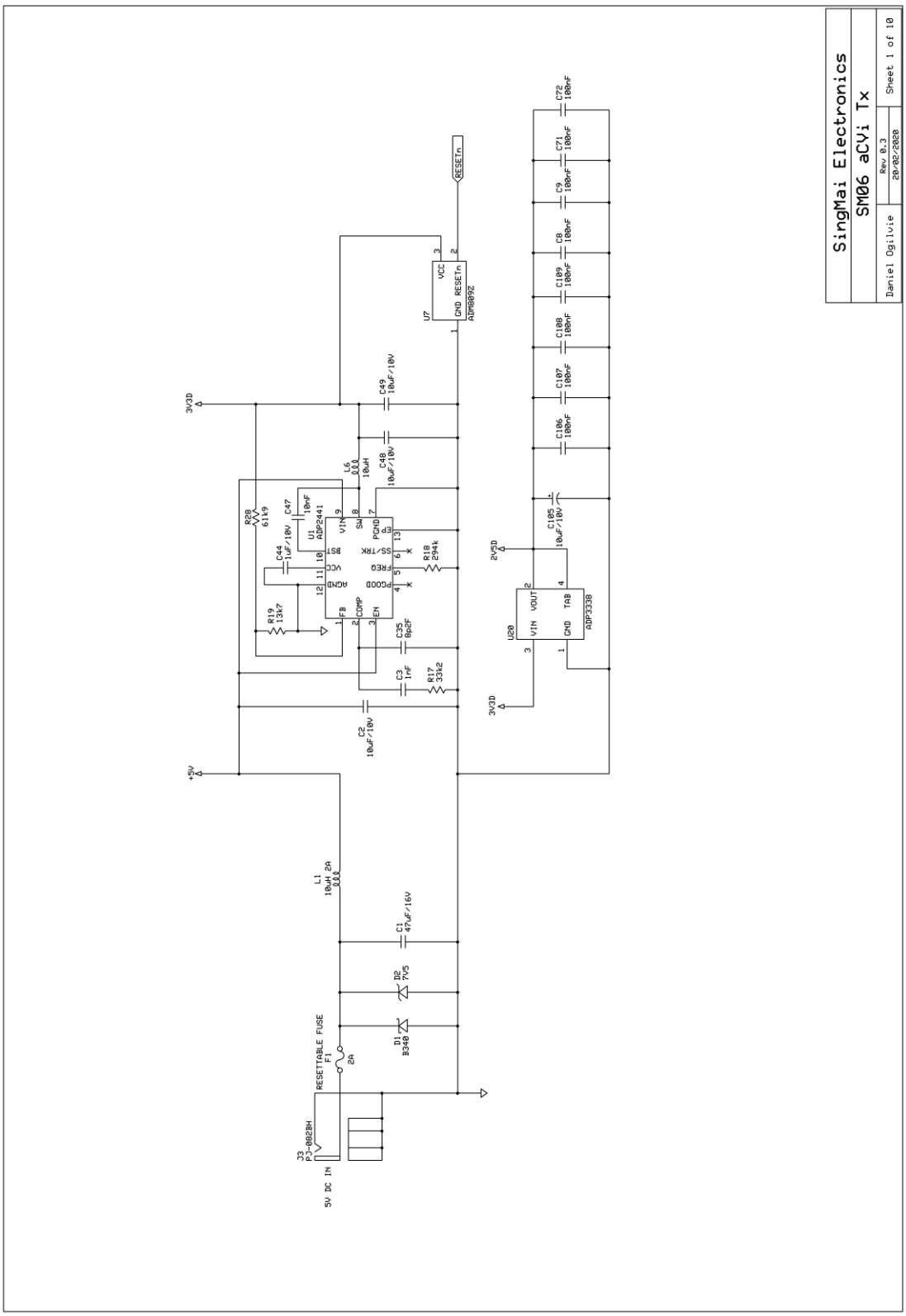

Figure 10 SM06 Schematics - Sheet 1.

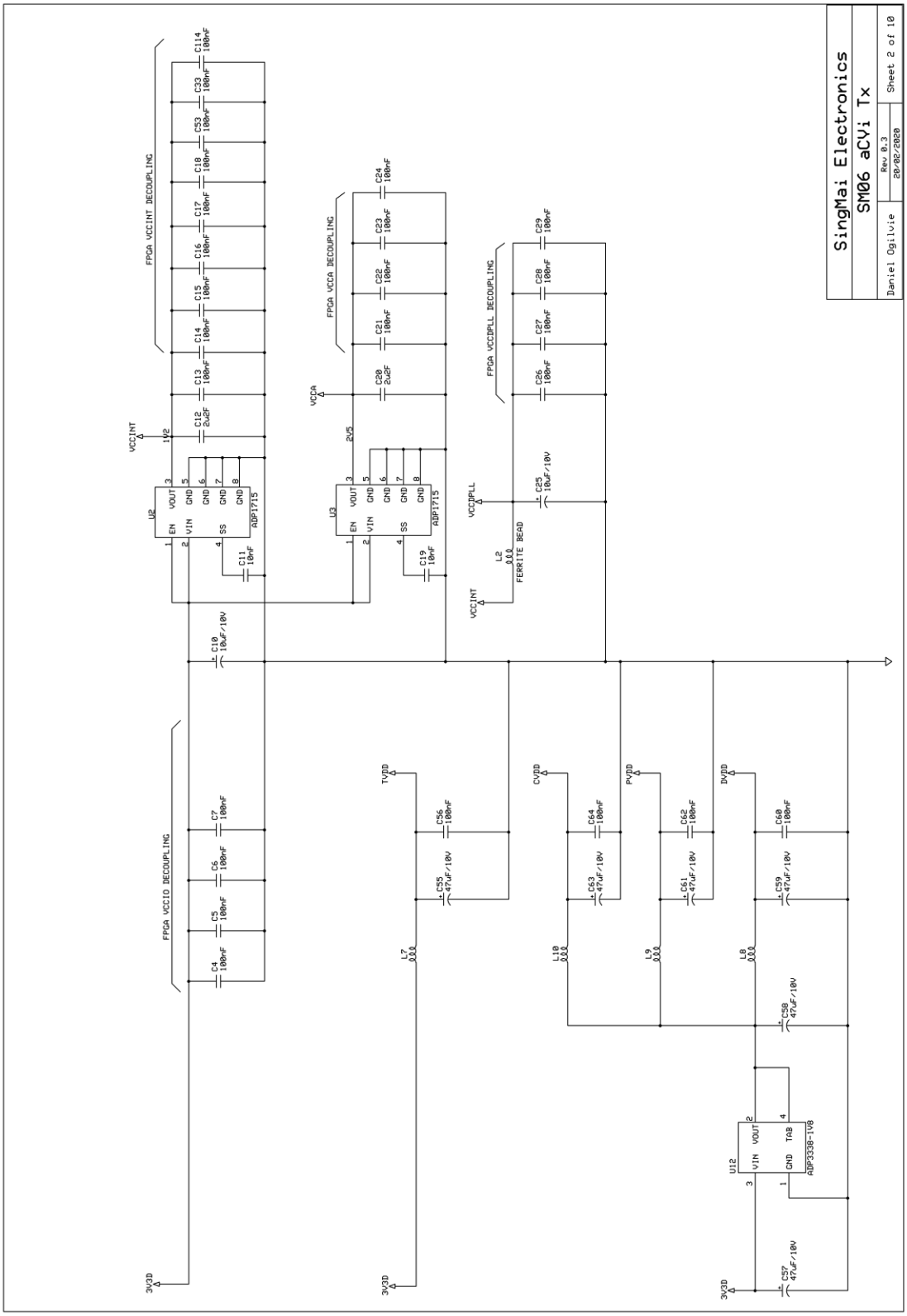

Figure 11 SM06 Schematics - Sheet 2.

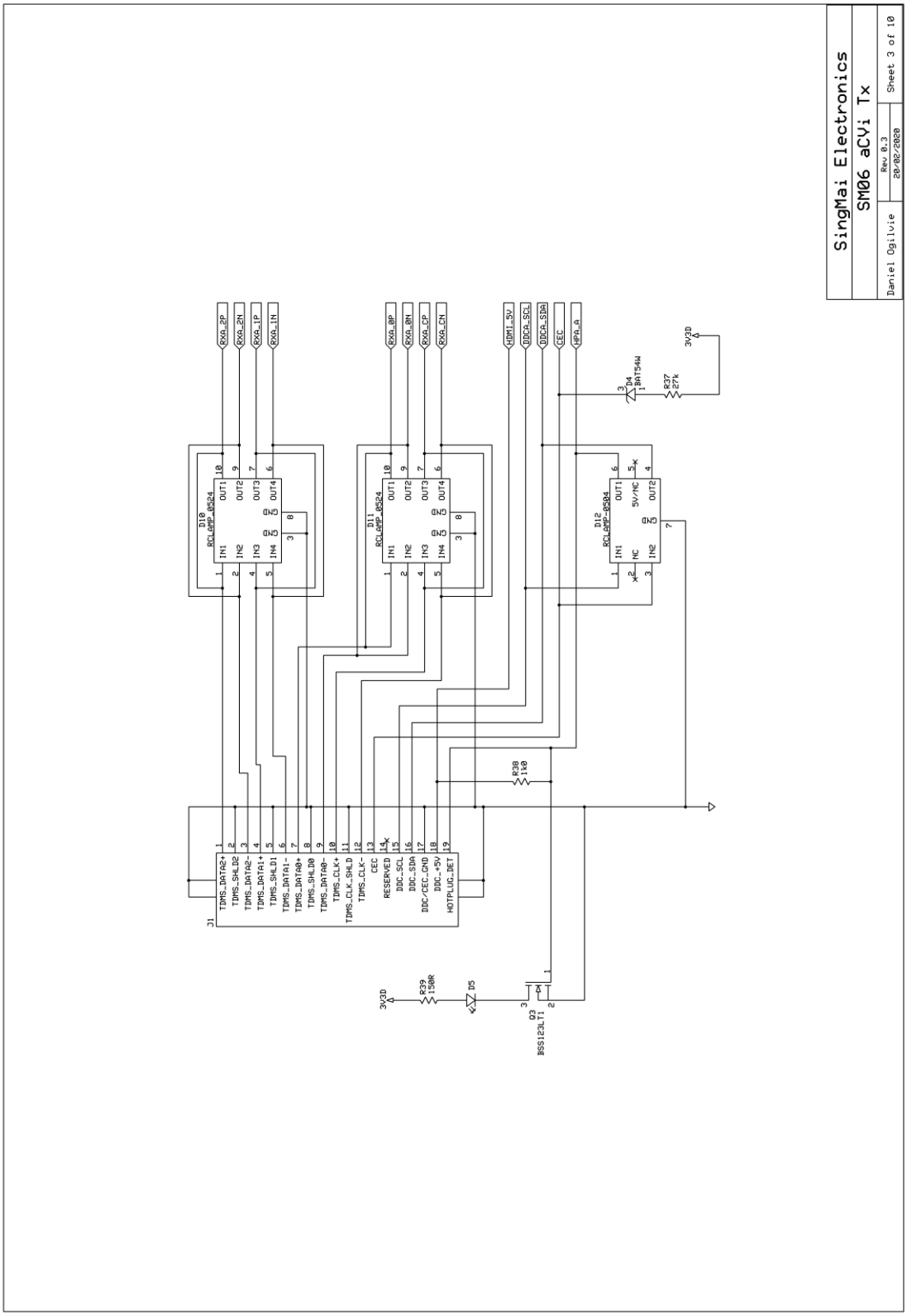

Figure 12 SM06 Schematics - Sheet 3.

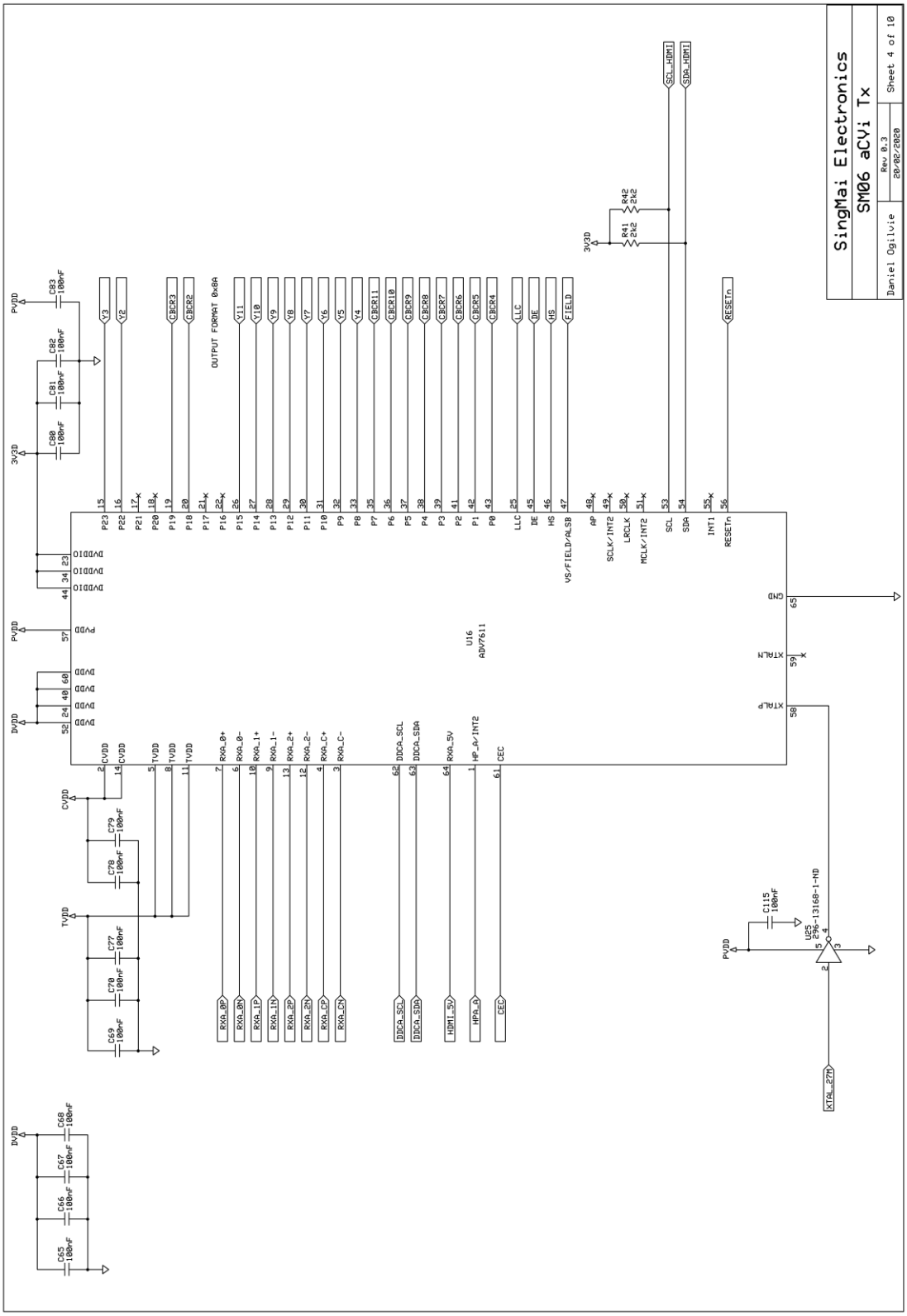

Figure 13 SM06 Schematics - Sheet 4.

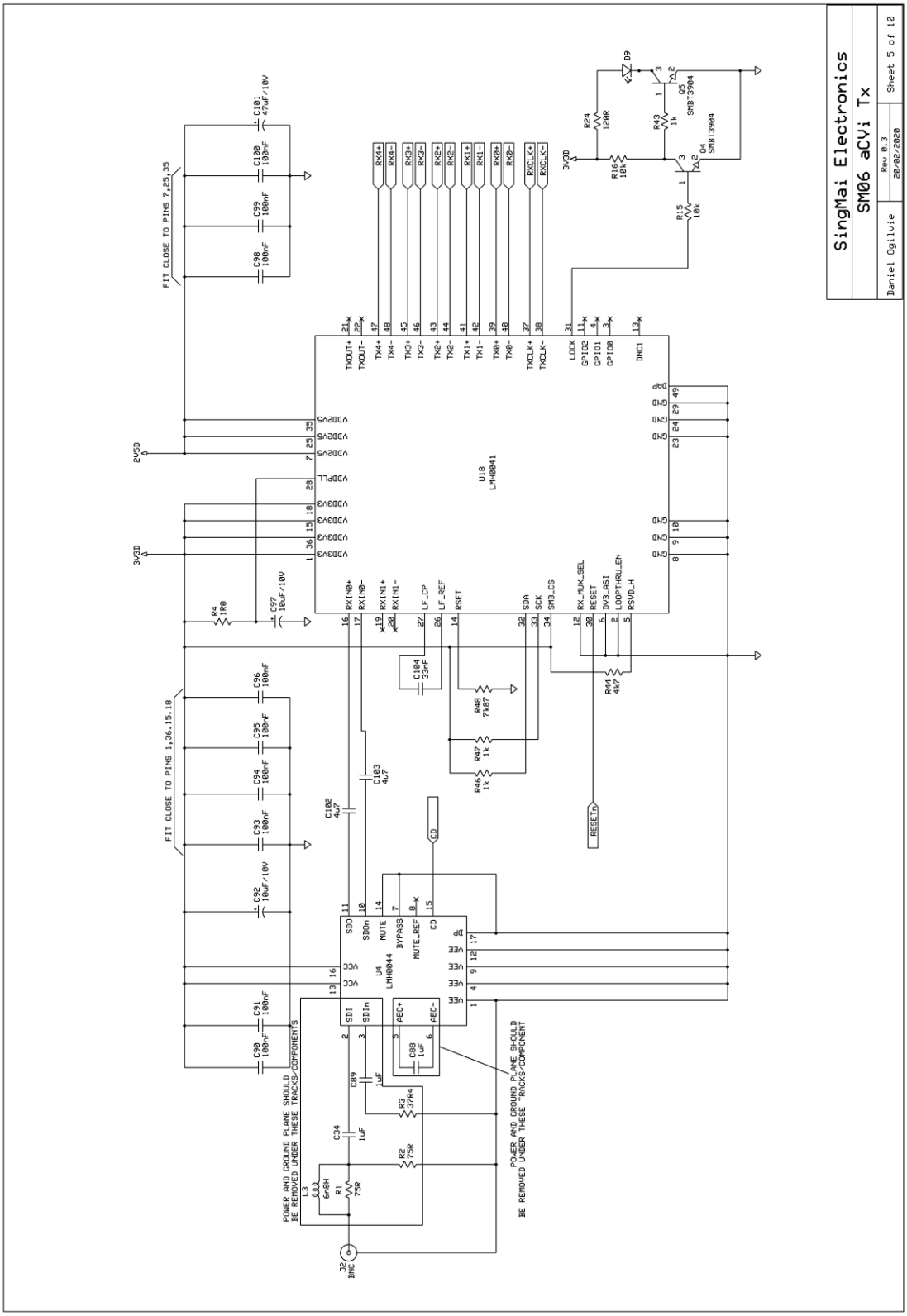

Figure 14 SM06 Schematics - Sheet 5.

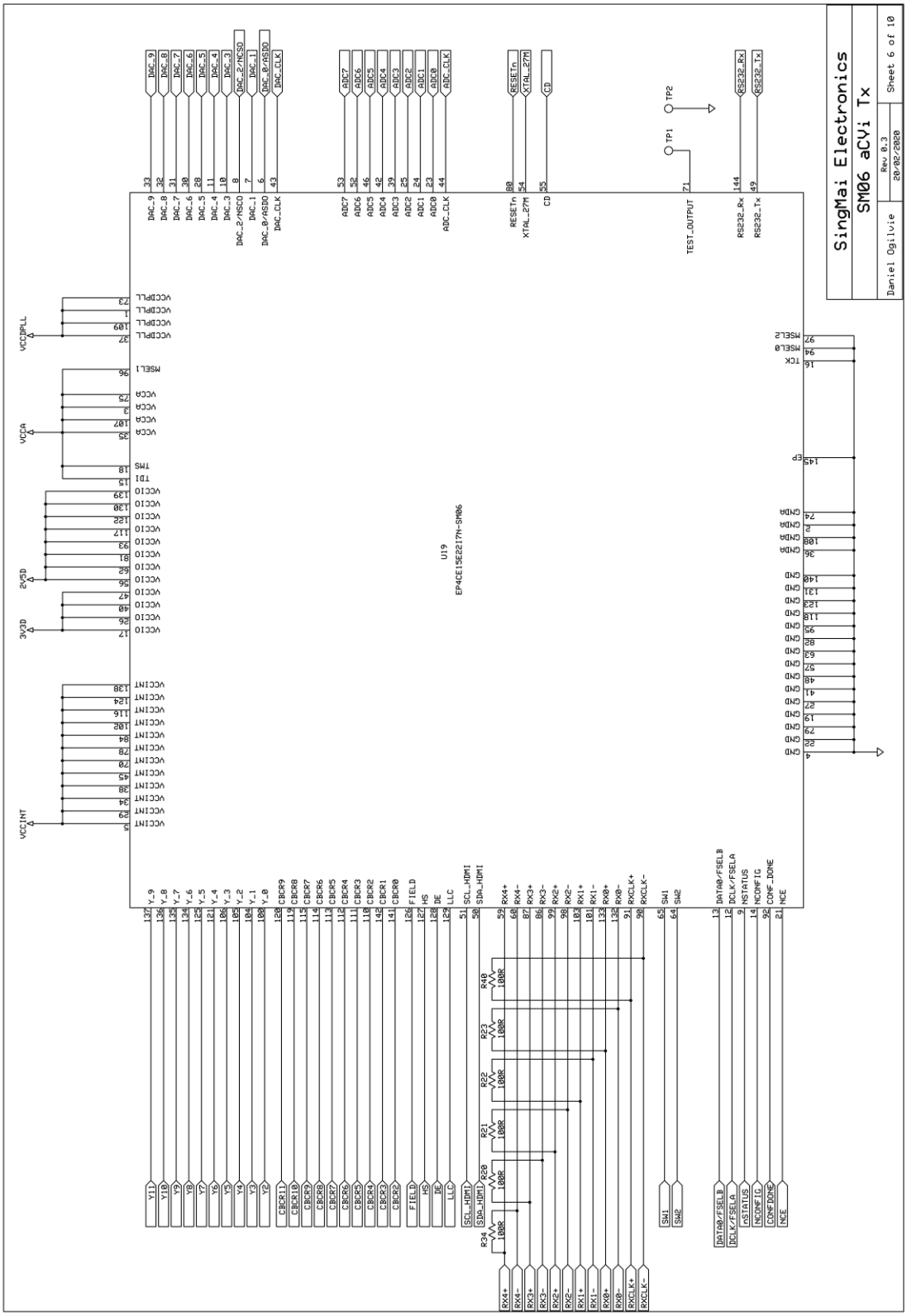

Figure 15 SM06 Schematics - Sheet 6.

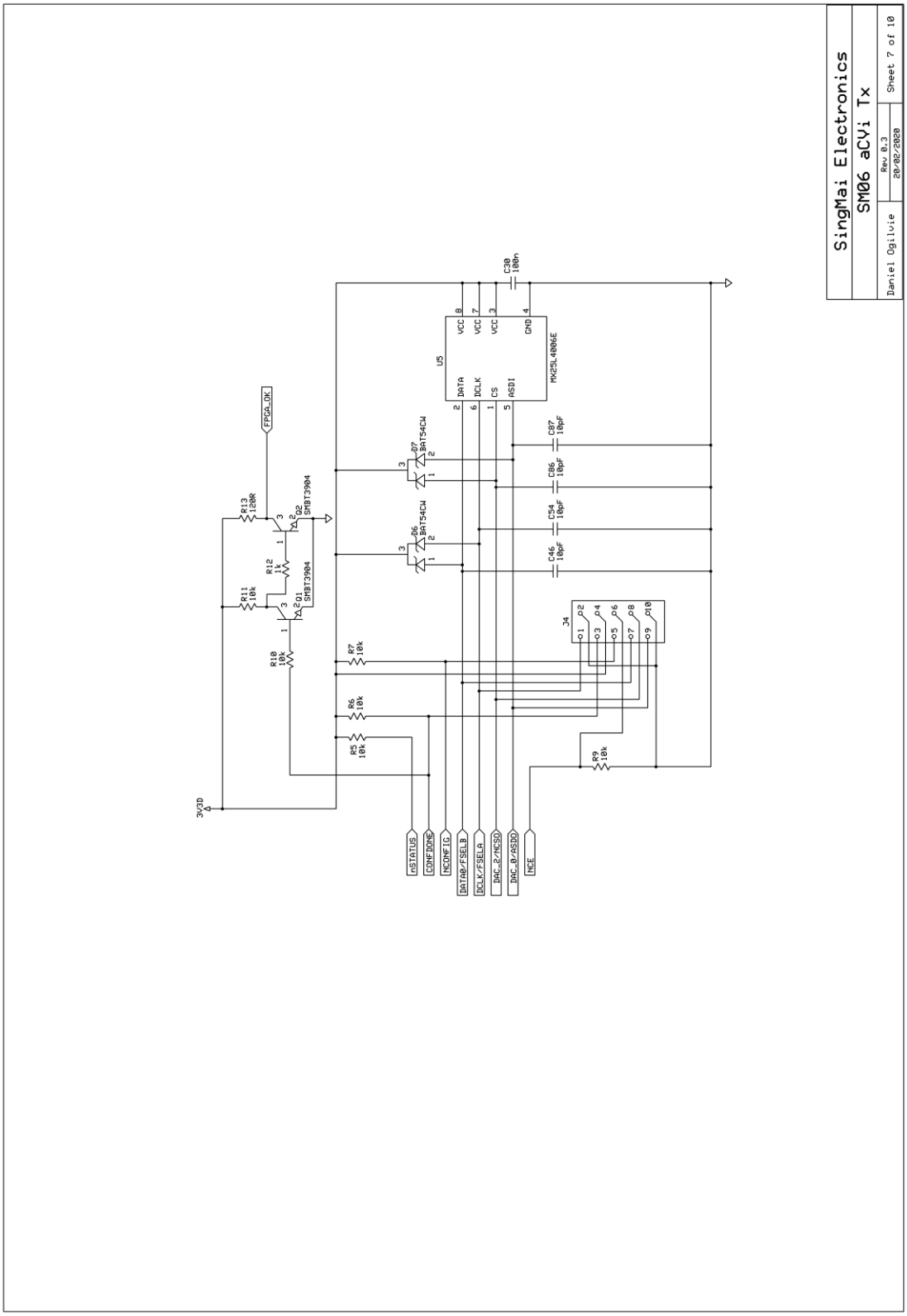

Figure 16 SM06 Schematics - Sheet 7.

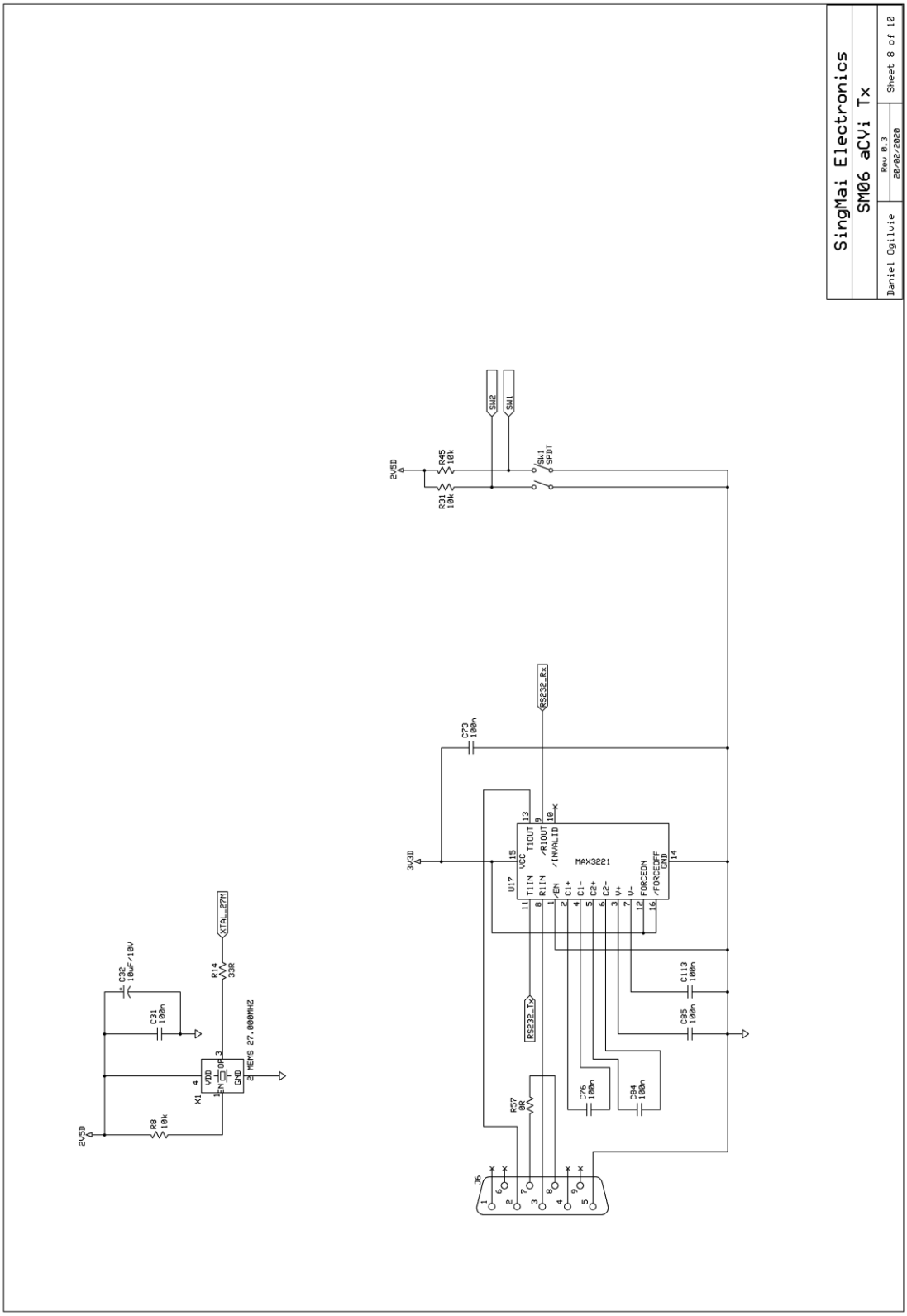

Figure 17 SM06 Schematics - Sheet 8.

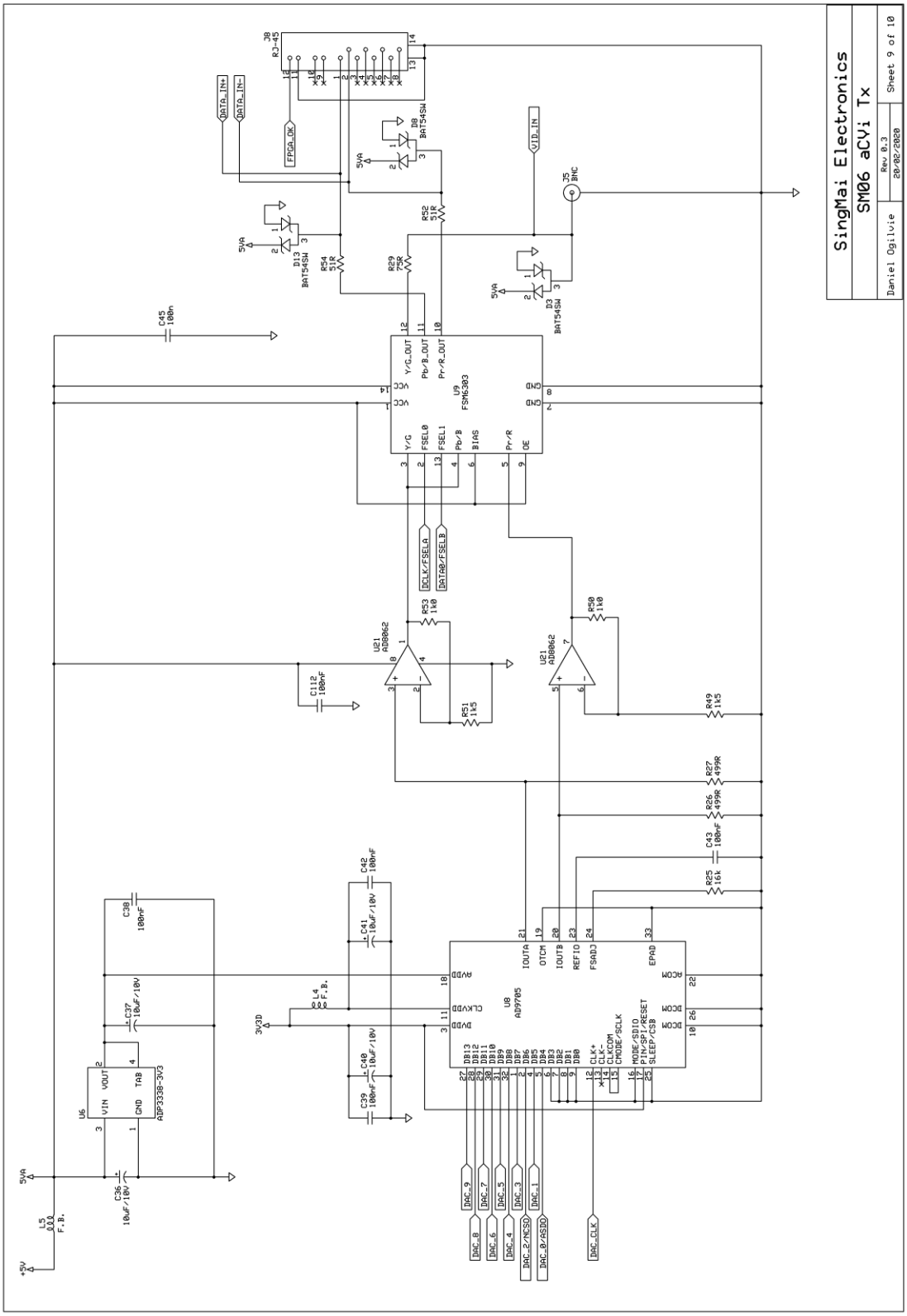

Figure 18 SM06 Schematics - Sheet 9.

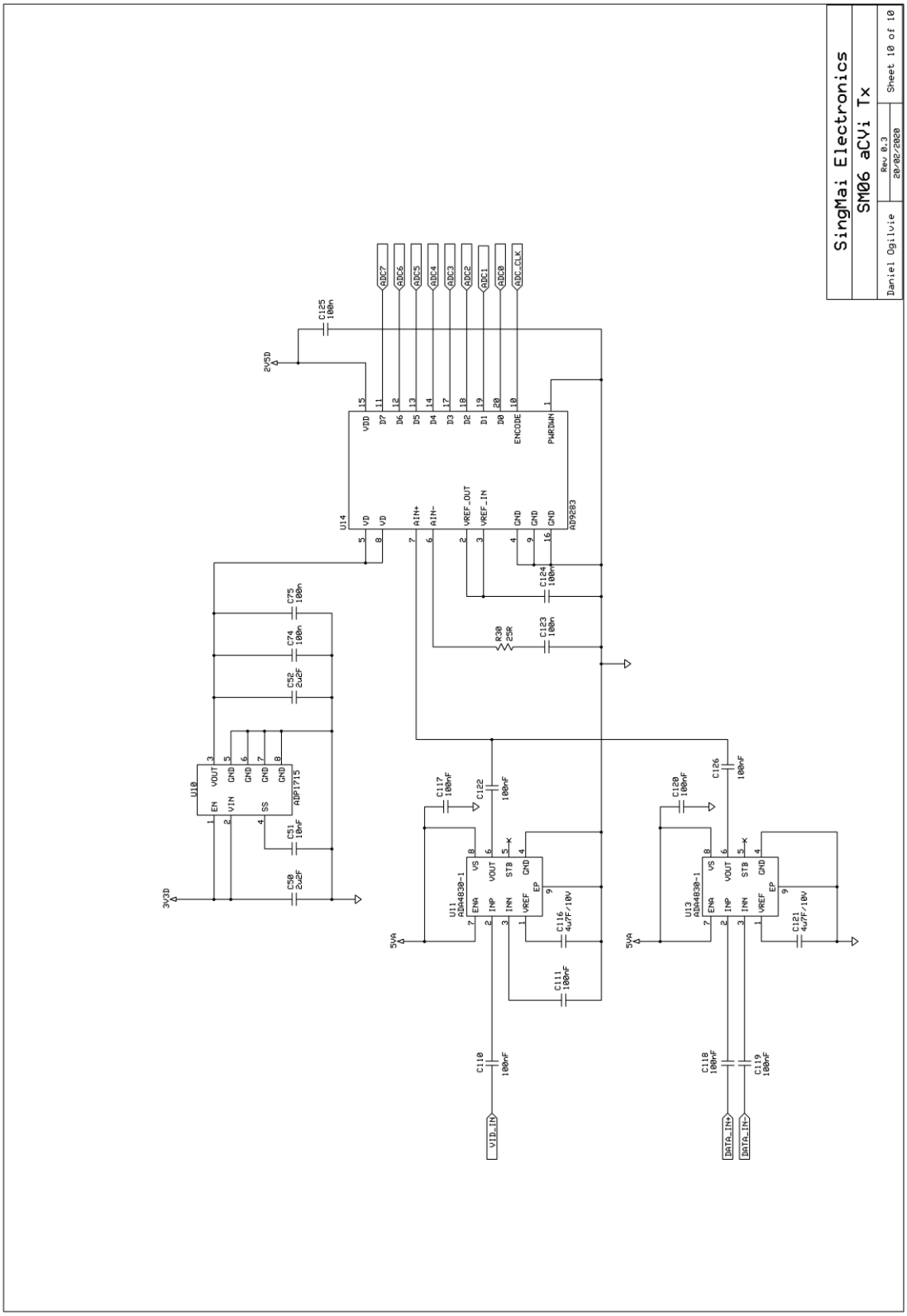

Figure 19 SM06 Schematics - Sheet 10.