SM08

Advanced Composite Video Interface:

aCVi Receiver module

User Manual

Revision 0.1
17th April 2022

Revision History

Date	Revisions	Version
14-10-2021	First Draft.	0.1

Contents

Figures

1. Introduction

aCVi® is SingMai's proprietary interface for transmitting high-definition video over long distances of coaxial or twisted-pair cable.

SM08 is a receiver module compatible with the aCVi® Advanced Composite Video Interface format. SM08 accepts analogue aCVi® encoded video from both twisted pair and low-cost coaxial cable which it converts to HD-SDI format video.

SM08 supports the following HD standards: 720p-23/24/25/29/30/50/59/60Hz, 1080p-23/24/25/29.97/30Hz and 1080i-50/59.94/60Hz. Switching between standards is automatic.

Figure 1 SM08 module.

The compatible aCVi® transmitter for the SM08 receiver is the **SM06** (HD-SDI input).

Other aCVi® modules/boards include:

PT56 aCVi encoder IP core.

PT52 aCVi decoder IP core.

SM02 aCVi video test pattern generator.

SM07 aCVi camera module

For the latest list of available modules follow **this link**. (https://www.singmai.com/aCVi.html)

2. aCVi Overview

The following is a brief overview of the aCVi® revision 2 interface (abbreviated to aCVi® in this document).

aCVi® is a proprietary format, developed by SingMai Electronics, to transmit high definition video over long distances of coaxial or twisted pair cable. aCVi® is an update to the previous version, specifically designed to interface directly to image sensors, although it may also be used to transmit conventional video sources.

A single chip image sensor, as found in almost all non-broadcast cameras, uses a colour filter to 'assign' each sensor pixel one of red, green or blue sensitivities. Because green is where the human eye is most sensitive, there are twice as many green pixels as red and blue (see Figure 2). This means that if your sensor has a horizontal array of 1920 pixels, only 960 of them are green, red or blue pixels, and for the red and blue pixels, each horizontal line is either red or blue. So, the actual resolution of the sensor to each colour is for green, 960 x 1080 pixels, and for red and blue, 960 x 540 pixels. (A broadcast camera will use three optically aligned sensors, each offering 1920 x 1080 pixels for the three colours). If we refer to the full resolution as 4:4:4 sampled, a single image sensor actually produces a 2:2:0 output.

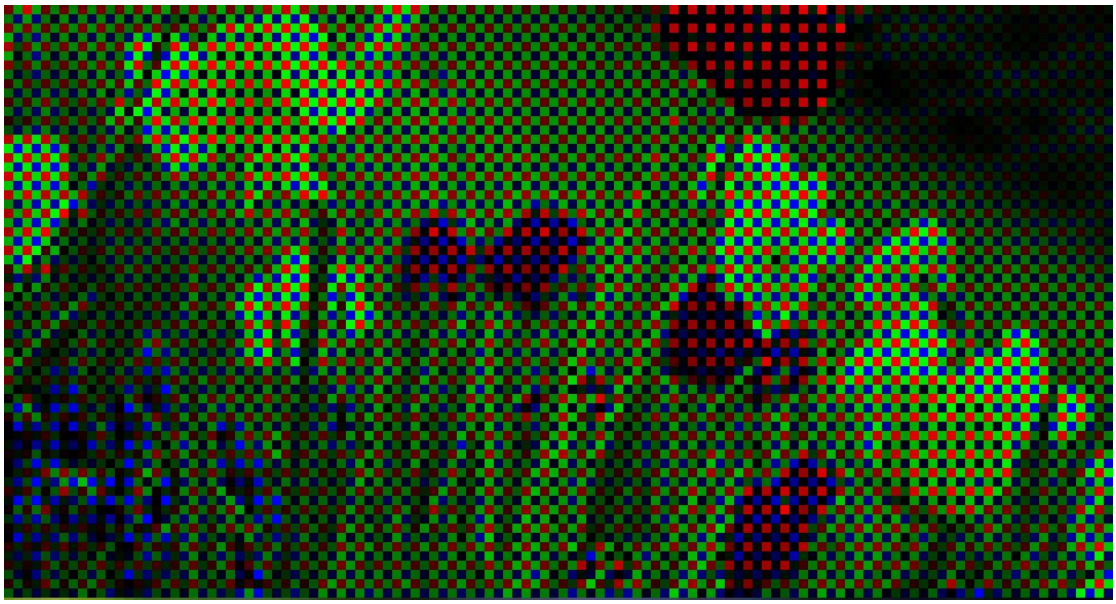


Figure 2 Bayer colour filter.

To conform with video standards (e.g. 1920 x 1080) the additional pixels are interpolated (a technique known as Bayer de-mosaicing) and this function is usually performed in the camera ISP (Image Signal Processor). However, this process can produce artifacts into the image (for example see the colour artifacts on the white fence in Figure 3), and also, because it generates more than double the number of original pixels, more than doubles the bandwidth of the output signal, which exacerbates the problem if the video is required to transmitted long distances.

aCVi® interfaces directly to the single chip image sensor and transmits the RAW 2:2:0 resolution image directly, thereby reducing by more than half the bandwidth of the transmitted signal and achieving higher resolution, lower noise and greater distances.

Figure 3 Left: Original full resolution image. Right: Image after Bayer demosaicing.

If required, aCVi® may transmit bi-directional data and the interface is also compatible with power over coax.

The available aCVi® modules are shown in Figure 4. SM07 is an aCVi® camera module which uses a high-definition Sony sensor. The SM06 provides an aCVi® transmitter for HD-SDI video sources and simultaneously drives both coaxial and twisted-pair cable.

The receiver module is the SM08. This module accepts either twisted-pair or coaxial cable and converts the aCVi® video to an HD-SDI output for a TV monitor or video recorder.

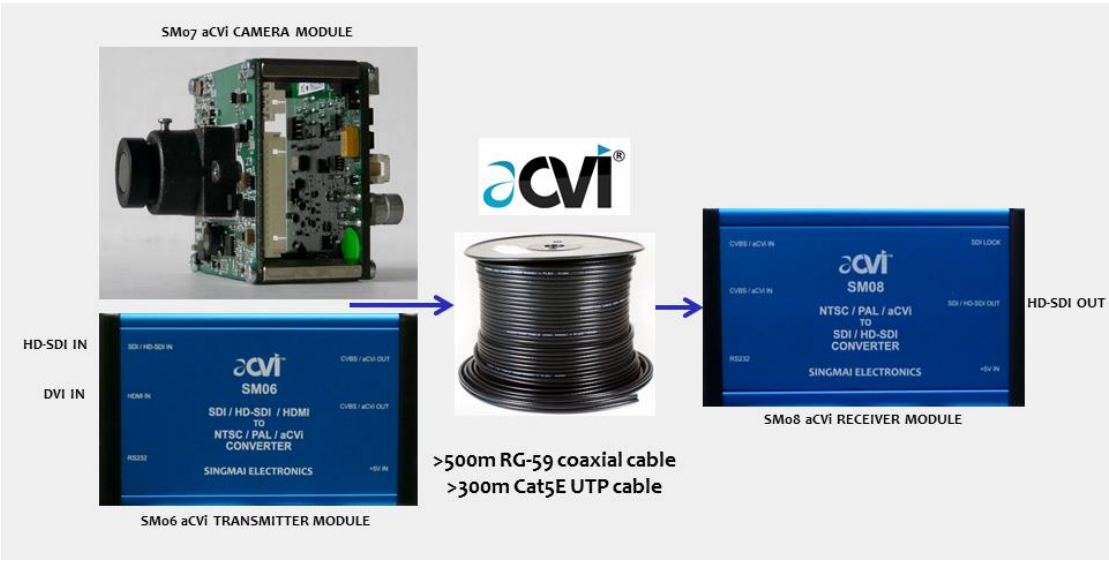


Figure 4 aCVi Modules.

aCVi® is designed to interface directly to the image sensor. Functions of the ISP are limited to missing pixel detection, black level restoration, auto iris (if required) etc. and these are integrated into the aCVi® transmitter, **negating the need for a conventional camera ISP**. The RAW red, green and blue data from the image sensor is transmitted directly with no requirement for the Bayer de-mosaicing, and thereby halving the required transmission bandwidth with no additional artifacts being transmitted.

Because the RAW image data only needs to simultaneously transmit green and either red or blue, we can modulate this data onto to a single carrier in quadrature. For video standards up to 1080p/30Hz (74.25MHz sampling) we only need a bandwidth of 15MHz to retain full resolution from the sensor. The synchronization signals are sent on a (non-mathematically related) carrier. The spectrum of the aCVi® signal is shown in Figure 5. The full image sensor resolution can therefore be sent within a 37MHz bandwidth, allowing relatively low-cost ADCs and DACs.

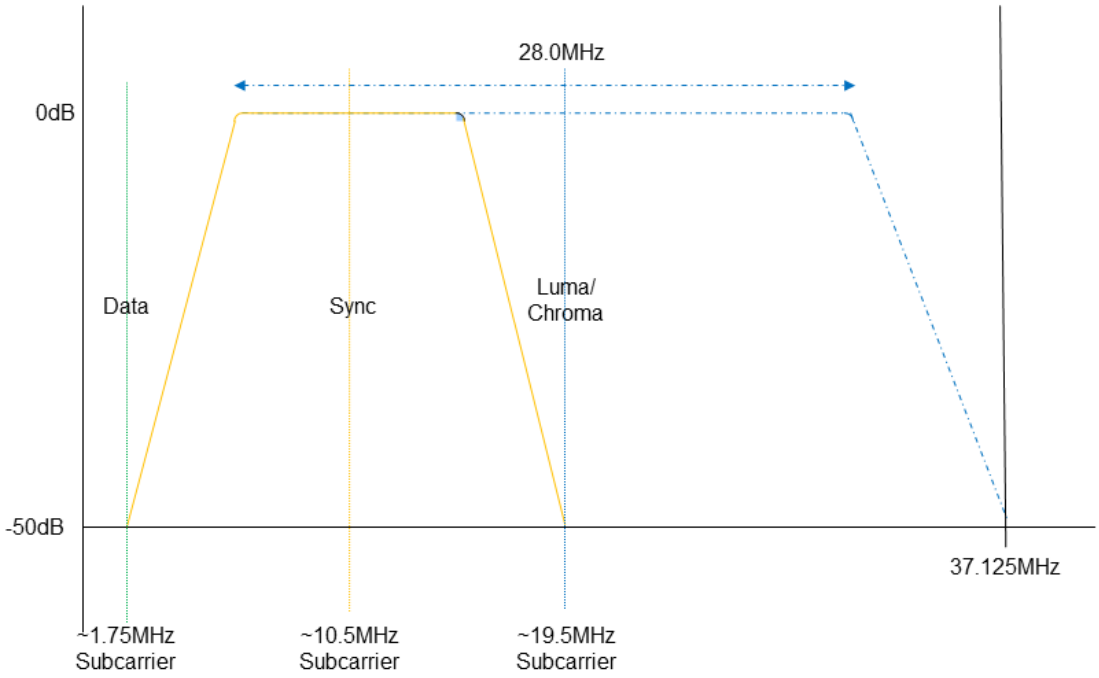


Figure 5 aCVi® Spectrum.

aCVi® also has provision for another low frequency carrier for data to be sent from the receiver to the transmitter, for example for camera control functions such as pan and tilt. The modulation method employed by aCVi® means that there is no low frequency or DC component to the signal, allowing power-over-coaxial to be employed. Also, the receiver analogue front end can be simplified as the signal can be AC coupled with no requirement for clamping.

The output of the aCVi® receiver is 2:2:2 sampled RGB. This can be recorded directly by the MPEG encoder (either as 2:2:2 or 2:2:0) thereby halving the amount of data that needs to be recorded for the same image quality (or better image quality as we have less artifacts and noise) and doubling the recorded time for the same bit rate and memory size. The only requirement for image conversion is for display (because of monitor compatibility reasons); image processing (feature analysis such as number plate or face recognition) can be performed on the RAW data.

aCVi® is also compatible with 'conventional' video input formats where it is not interfaced directly to an image sensor and this is the interface employed by the SM02. In this case the luma (Y) signal is bandwidth limited to 15MHz, and the R-Y and B-Y signals (also at 15MHz bandwidth) are sent line-sequentially.

The supported aCVi® video formats are shown in Table 1.

Standard	Pixels/line	Line frequency	Clock frequency	Horizontal sync width (clocks)	Broad pulse start position (clocks)	Broad pulse end position (clocks)	Burst gate start position (clock periods)	Video Subcarrier frequency	Sync Subcarrier frequency
720p/23Hz	4125	17.982kHz	74.18MHz	80	296	3755	151	19.465534MHz	10.471528MHz
720p/24Hz	4125	18.000kHz	74.25MHz	80	296	3755	151	19.503MHz	10.500000MHz
720p/25Hz	3960	18.750kHz	74.25MHz	80	296	3590	151	19.509375MHz	10.50625MHz
720p/29Hz	3300	22.477kHz	74.18MHz	80	296	2930	151	19.454296MHz	10.482018MHz
720p/30Hz	3300	22.500kHz	74.25MHz	80	296	2930	151	19.49625MHz	10.500000MHz
720p/50Hz	1980	37.500kHz	74.25MHz	80	296	1610	151	19.51875MHz	10.5125MHz
720p/59Hz	1650	44.955kHz	74.18MHz	80	296	1280	151	19.420579MHz	10.489510MHz
720p/60Hz	1650	45.000kHz	74.25MHz	80	296	1280	151	19.5075MHz	10.500000MHz
1080p/23Hz	2750	26.973kHz	74.18MHz	80	236	1920	121	19.461039MHz	10.474525MHz
1080p/24Hz	2750	27.000kHz	74.25MHz	80	236	1920	121	19.5075MHz	10.485MHz
1080p/25Hz	2640	28.125kHz	74.25MHz	80	236	1920	121	19.5046875MHz	10.500000MHz
1080p/29Hz	2200	33.716kHz	74.18MHz	80	236	1920	121	19.471154MHz	10.463287MHz
1080p/30Hz	2200	33.750kHz	74.25MHz	80	236	1920	121	19.490625MHz	10.5075MHz
1080i/50Hz	2640	28.125kHz	74.25MHz	80	236	1060	121	19.5046875MHz	10.500000MHz
1080i/59Hz	2200	33.716kHz	74.18MHz	80	236	1060	121	19.471154MHz	10.463287MHz
1080i/60Hz	2200	33.750kHz	74.25MHz	80	236	1060	121	19.490625MHz	10.5075MHz

Table 1 aCVi® supported video standards.

Standard	Pixels/line	Equalising Pulse width (clocks)	Half line start position (clocks)	2nd Sync width (clocks)	2nd Broad pulse start position (clocks)	2nd Broad pulse end position (clocks)
1080i/50Hz	2640	80	1320	80	1556	2380
1080i/59Hz	2200	80	1100	80	1326	2150
1080i/60Hz	2200	80	1100	80	1326	2150

Table 2 aCVi® supported video standards (interlaced standards).

3. Connecting up the module

The SM08 module is powered by a universal input (90-260VAC) AC-DC adaptor (see Appendix A for the power supply specification). The 5VDC, 12W output of this adaptor should be connected to the jack input, '+5V IN', of the SM08. Once connected, the green LED, 'FPGA OK' should light, indicating the FPGA has been correctly configured and the module is running.

Figure 6 shows the interconnections for SM08.

Figure 6 SM08 Interconnections.

The video input is connected to either the coaxial BNC connector or the RJ-45 style twisted pair connector. Do not connect both cable type inputs at the same time. aCVi® assumes the UTP cable connections are 'straight' so both the transmitter and receiver use pin 1 for the 'VIDEO+' (non-inverted) signal, and pin 2 'VIDEO-' (inverted) signal.

If the aCVi® input is valid and can be locked to, the yellow 'Lock' LED will light – the SM08 automatically detects the input video standard. Once the aCVi® decoder has locked and is decoding the yellow 'SDI lock LED' should light, indicating the HD-SDI output is valid. The HD-SDI video can then be connected to video monitor or video recorder.

4. Circuit description

Figures 7-15 show the schematics for the SM08. Below is a brief technical description of the module.

Sheet 1.
J3 is the 5VDC power input connector to the SM08 module. The 5VDC is protected from over-voltage and reverse polarity inputs by D1, D2 and resettable fuse, F1. The input is then filtered by L1 and C2 to provide the 'clean' 5VDC for the analogue input stage and also linear regulated by U1 and U8 to provide the 3.3VDC and 2.5VDC supply voltages. U7 provides a power on reset for the FPGA.

Sheet 2.
U2 provides the 1.2VDC for the internal voltage of the FPGA. U3 provides the 2.5VDC for the analogue PLL circuity of the FPGA and L2 and C25 filter the VCCINT for the FPGA PLL digital blocks.

Sheet 3.
Sheet 3 is the analogue front end (AFE). The aCVi® analogue video inputs may be either coaxial or twisted pair.
If twisted pair, they are terminated in 100Ω (R26) and converted from differential to single ended outputs by U9. If coaxial inputs they are treated as a pseudo-differential input, with the ground screen of the BNC input connector connected to ground via R25 and C61, which affords some hum rejection for long cable runs. U15 converts this pseudo-differential input to a singled ended output. The two amplifier outputs are AC coupled and joined together; for this reason only one cable type input should be connected at one time.
U10 is a voltage-controlled amplifier. The aCVi® decoder measures the amplitude of the synchronizing signals and compares them to an internal reference: this amplifier compensates for the signal loss in the cable. The PWM Gain signal from the FPGA is low pass filtered and used to control the gain of U10.
The output of U10 is AC coupled into U11A, which is a high input impedance, low input bias current op-amp – U11B is not used for aCVi®. The AC coupled video is set the mid-point of the ADC operating range (1.5VDC - the ADC requires a 0.5V to 2.5V (2V pk-pk) input signal).

Sheet 4.
U19 is a dual 10 bit, 80MHz ADC. The ADC is used in single-ended mode. The clamped video from U11A is applied to the VIN+ input of both ADCs, and VIN- input is biased to mid rail (1.5V). U14 provides the 'clean' 3.0V supply for the ADC. The output of the ADC, ADC[9:0] is the 2's complement, digital composite video which is applied directly to the aCVi decoder. The two ADCs are clocked out of phase and the outputs multiplexed in the aCVi® decoder. This effectively produces a twice sample rate output (i.e. 74.25MHz clock produces a 148.5MHz data rate).

Sheet 5.
U4 is the FPGA. The FPGA is an Altera EP4CE15 device in a 144 pin 0.5mm TQFP package. The FPGA contains the PT52 aCVi® decoder, a SingMai PT13 control microprocessor and the HD-SDI output encoder.

Sheet 6.
The FPGA is a volatile device and needs configuring at switch on, which it does using U5, a 4Mb EEPROM. The device is automatically configured on switch on, and successful configuration is indicated by LED, 'FPGA OK'. The EEPROM may also be reprogrammed via J4, which is compatible with the Altera 'USB-Blaster' and the Quartus Programmer.

Sheet 7.
The PT52 aCVi decoder requires a line locked clock. This is achieved using a voltage-controlled crystal oscillator, with the frequency of the oscillator controlled using a PWM output from the PT52 IP core. This output, VCO_PWM, is filtered by R14 and C31 to provide an analogue voltage which is buffered by U6. The resulting 0-3.3V control voltage adjusts the frequency of the crystal voltage-controlled

oscillator (VCXO), X1. The adjustment range is approximately ±150ppm. The centre frequency (1.65VDC control voltage) is 27.0MHz.
The output of the VCXO is then multiplied to 74.25MHz or 74.18MHz (to provide support for 29.97/59.94Hz formats) – selection is performed via the FREQ_SEL.

The 'LOCK' LED is driven from a port of the FPGA. It is lit when the aCVi® decoder status indicates that horizontal lock has been achieved and the input is a valid standard supported by the decoder.

U17 is an RS232 level translator. The RS232 data interface is not enabled at this time.

Sheet 8.

This sheet is not currently fitted.

Sheet 9.

The Y, Cb and Cr video and the Hout, Vout and Fout synchronizing signals from the aCVi decoder are formatted into an HD-SDI signal inside the FPGA. The synchronizing signals are modified to be compatible with the HD-SDI Flag requirements and the line count is derived. The video and the timing signals (TRS) are combined and scrambled according to the HD-SDI specification and cyclic redundancy check (CRC) is added.
The scrambled signal is then multiplexed into 5 data streams at 148.5MHz which are driven as LVDS outputs, together with an LVDS clock, to the HD-SDI serialiser IC, U18, which converts these five data signals into one 1.485GHz, HD-SDI compatible, output (J9).

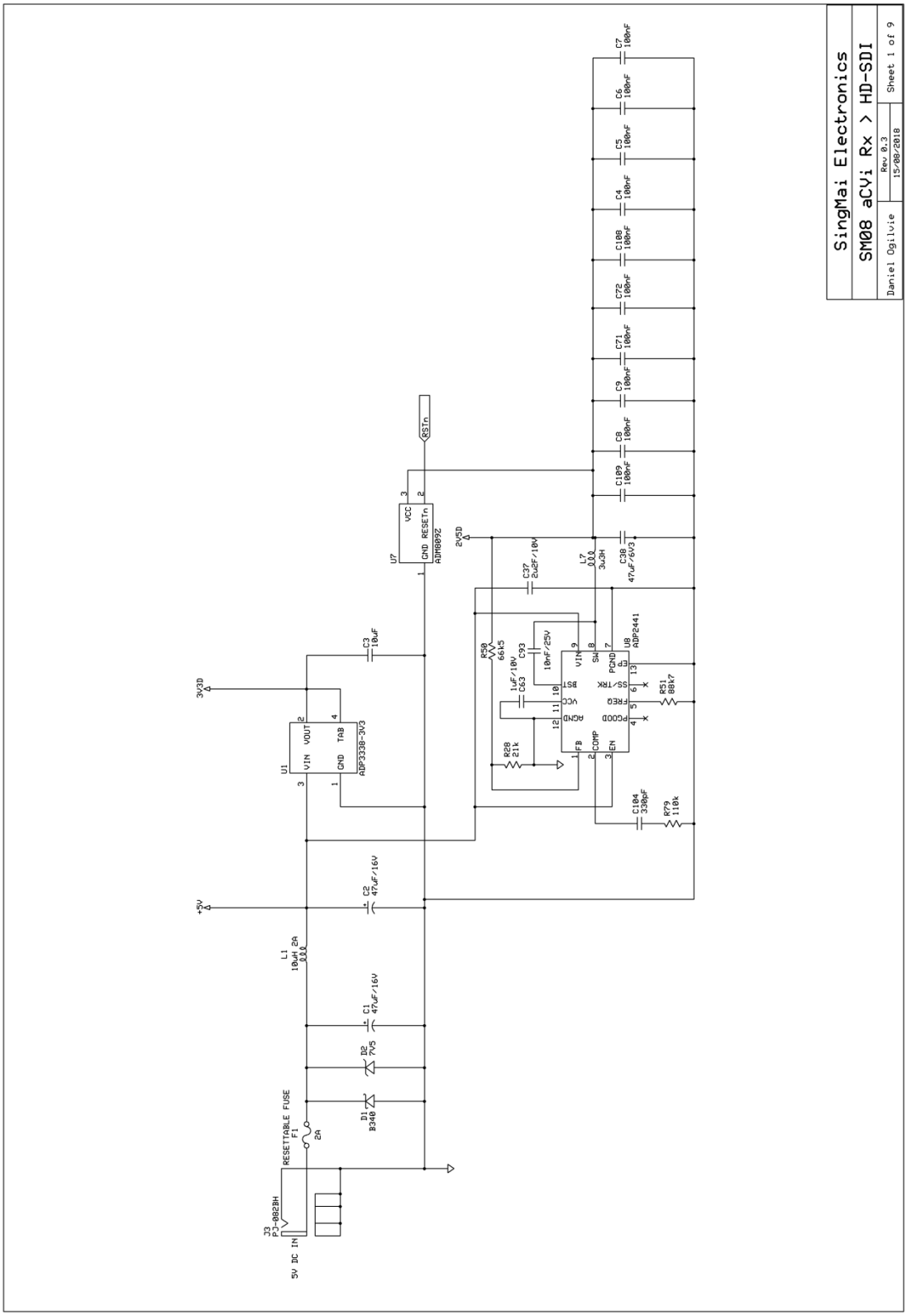


Figure 7 SM08 Schematics - Sheet 1.

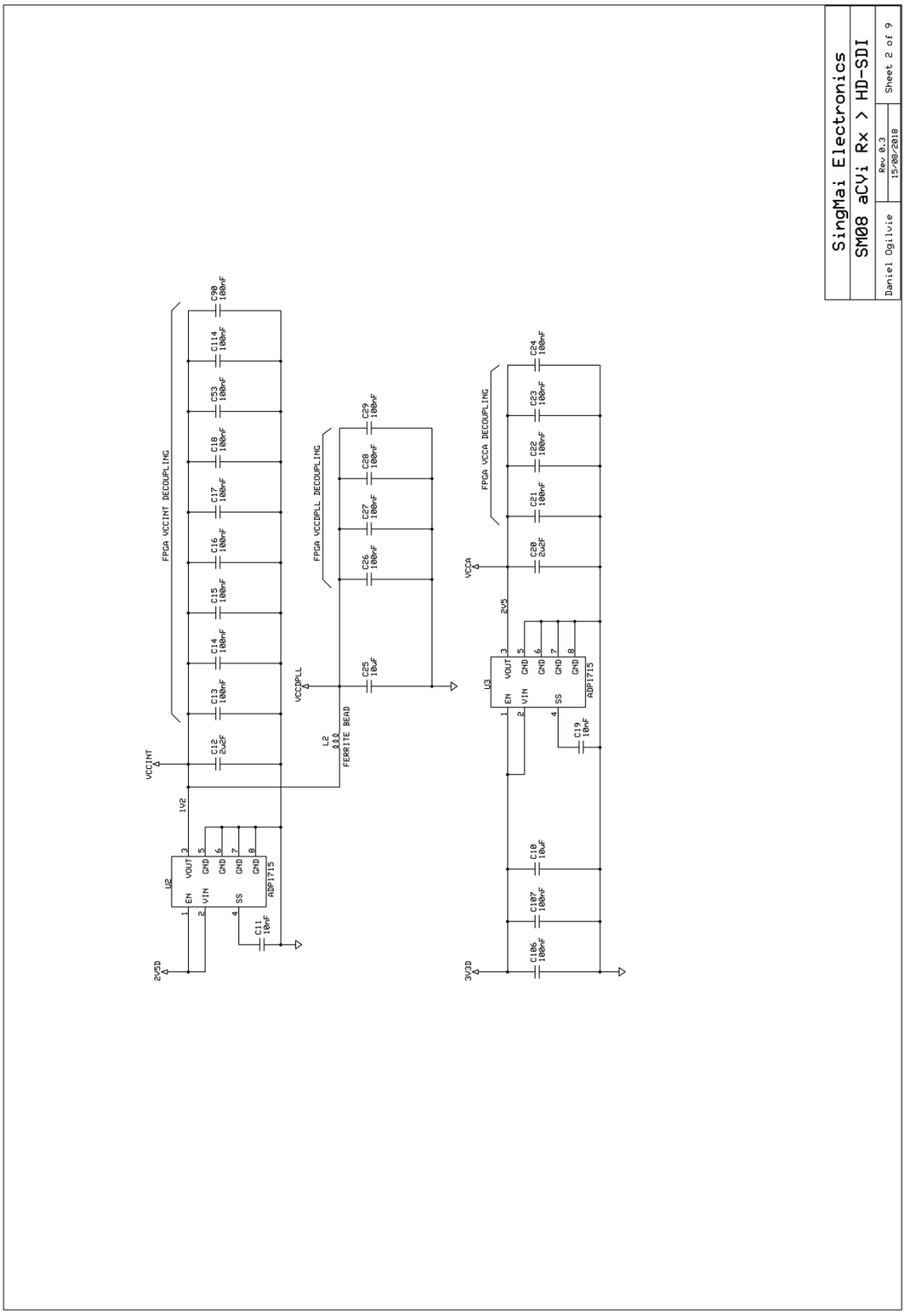


Figure 8 SM08 Schematics - Sheet 2.

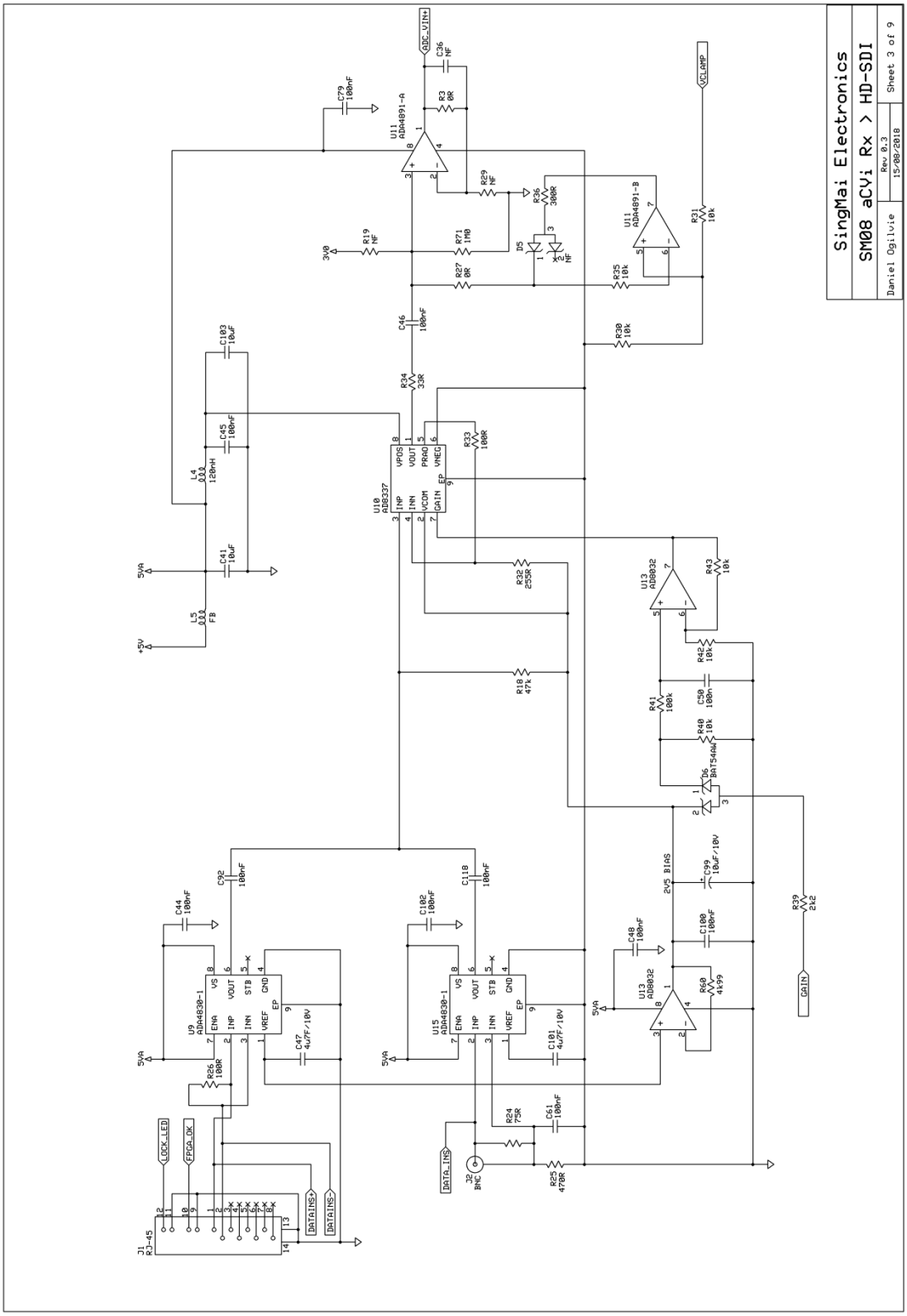


Figure 9 SM08 Schematics - Sheet 3.

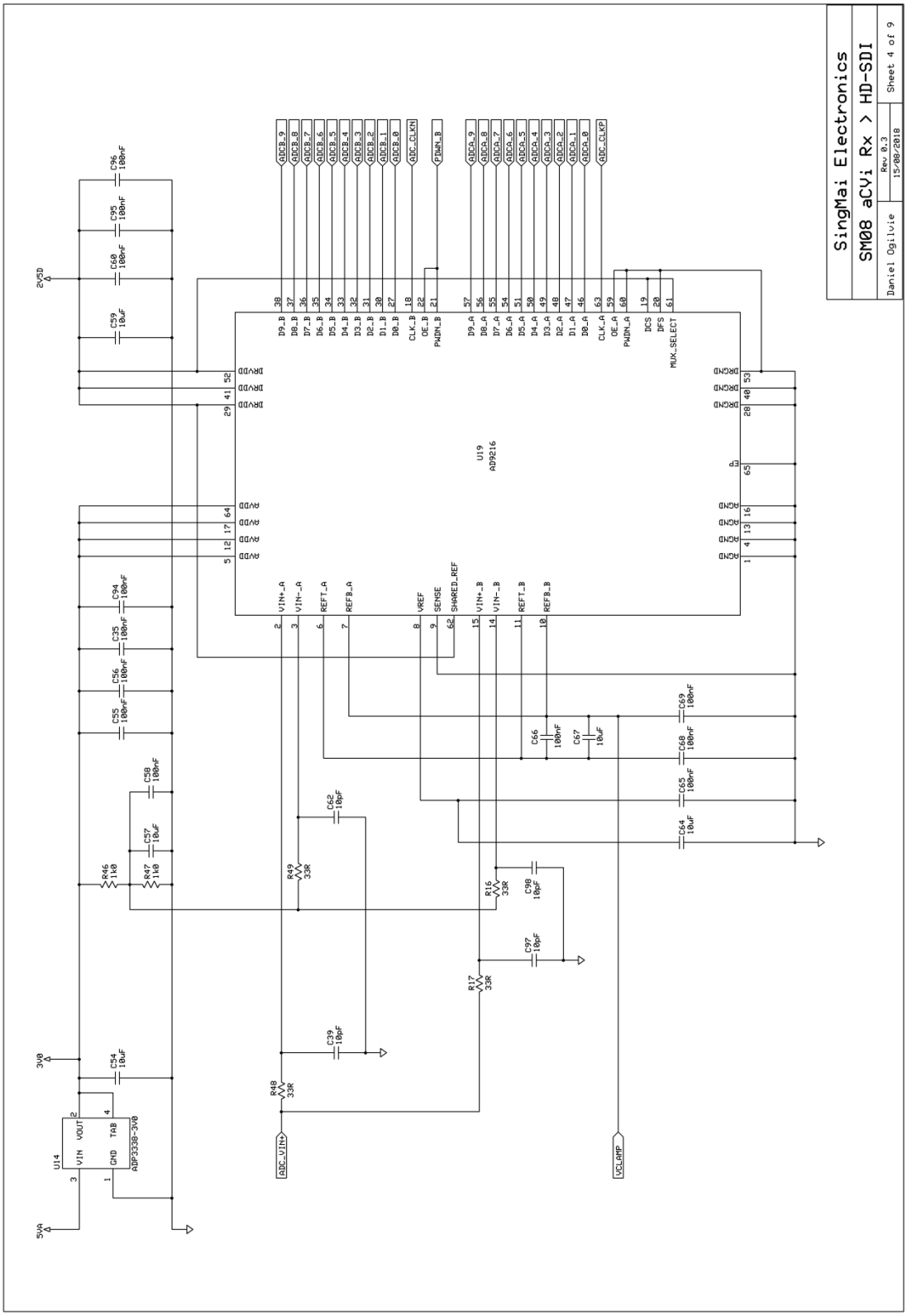


Figure 10 SM08 Schematics - Sheet 4.

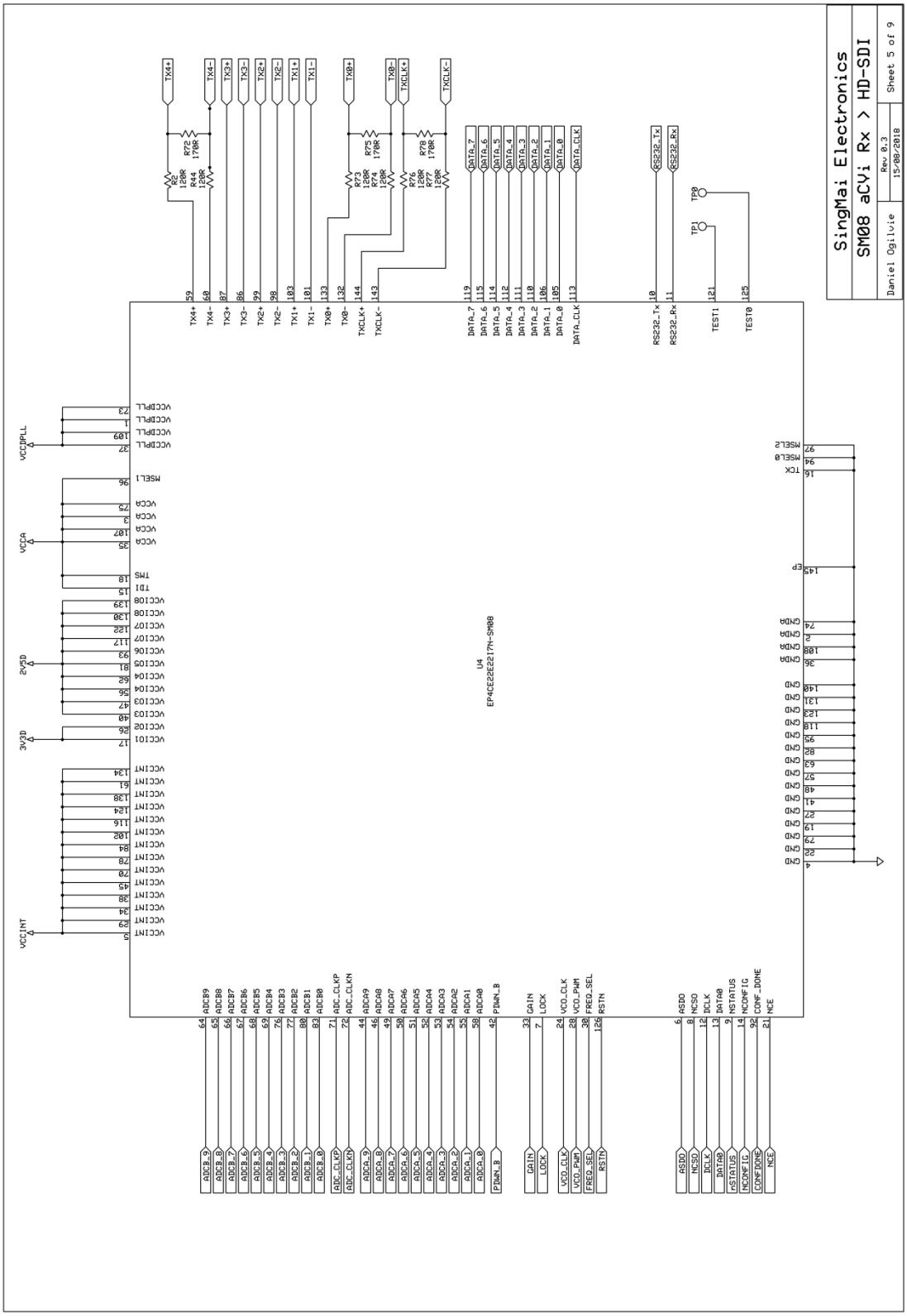


Figure 11 SM08 Schematics - Sheet 5.

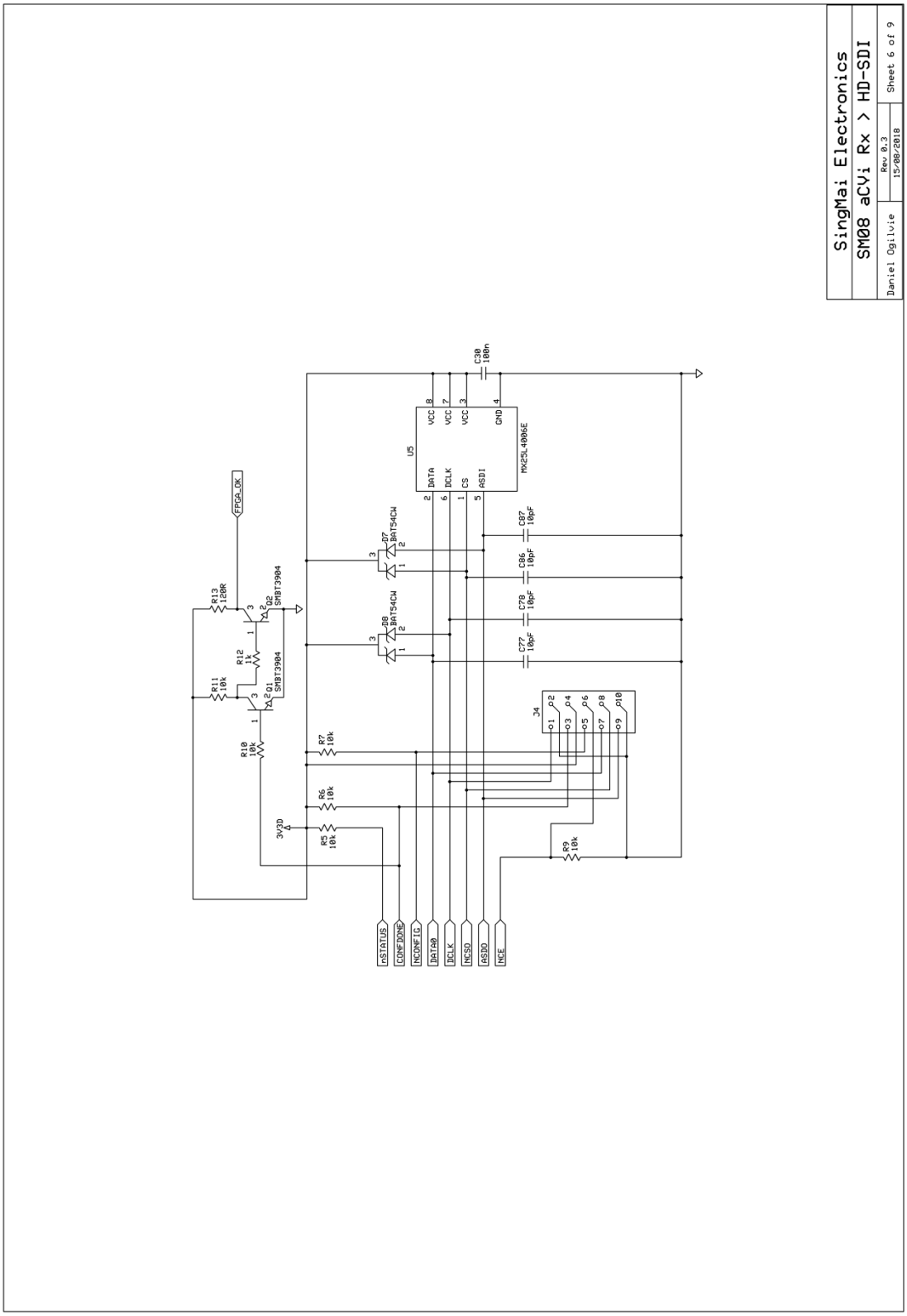


Figure 12 SM08 Schematics - Sheet 6.

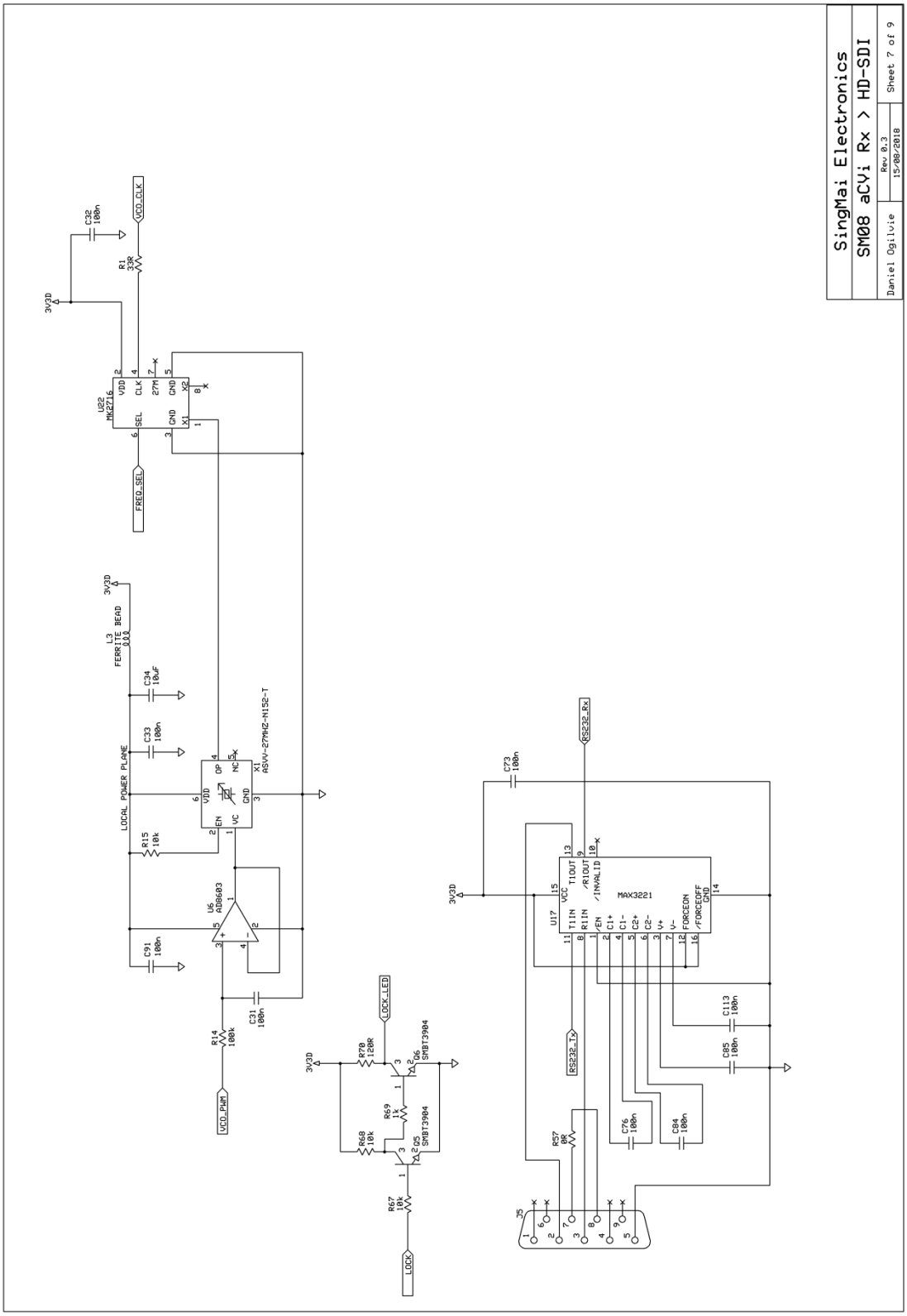


Figure 13 SM08 Schematics - Sheet 7.

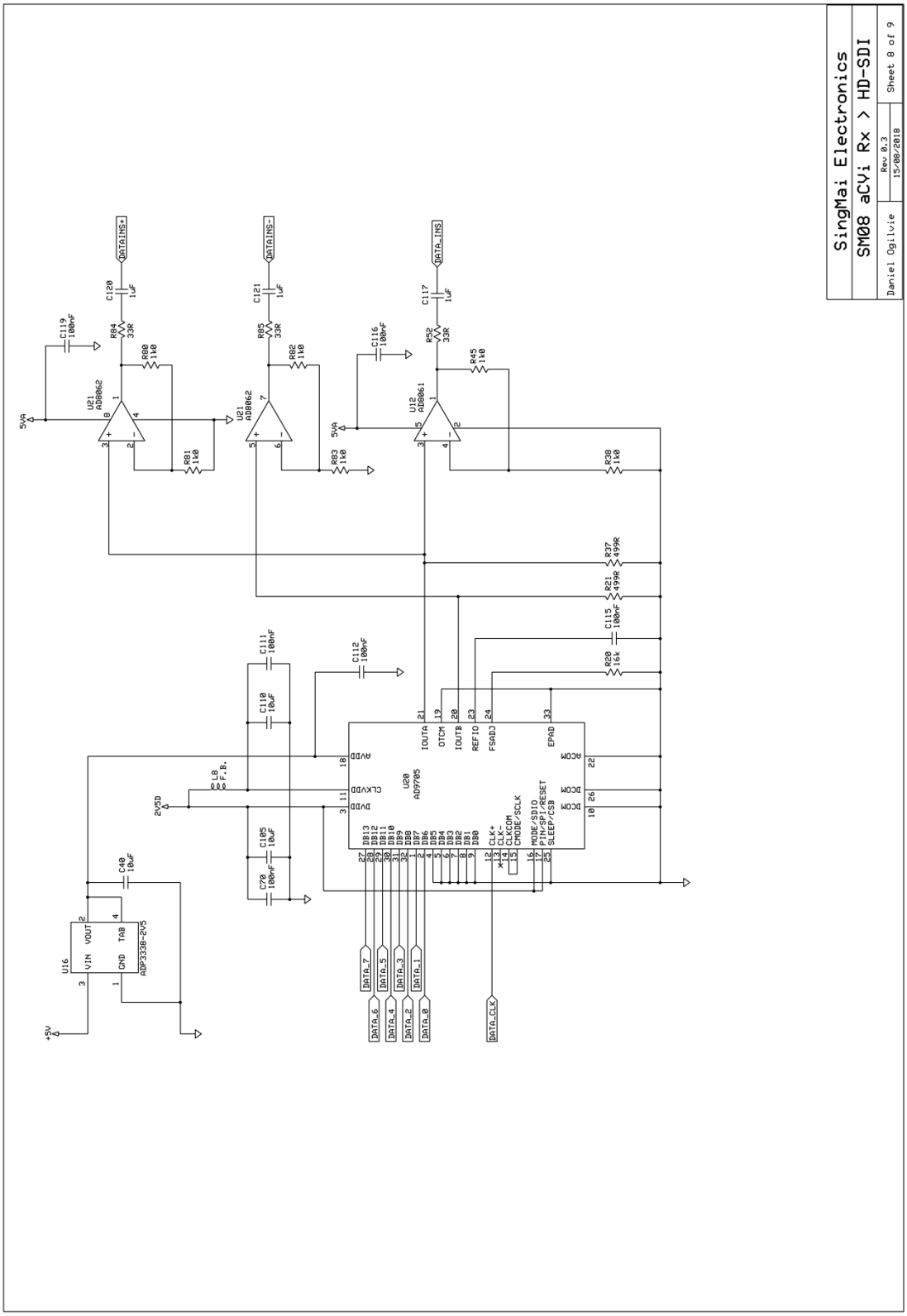


Figure 14 SM08 Schematics - Sheet 8.

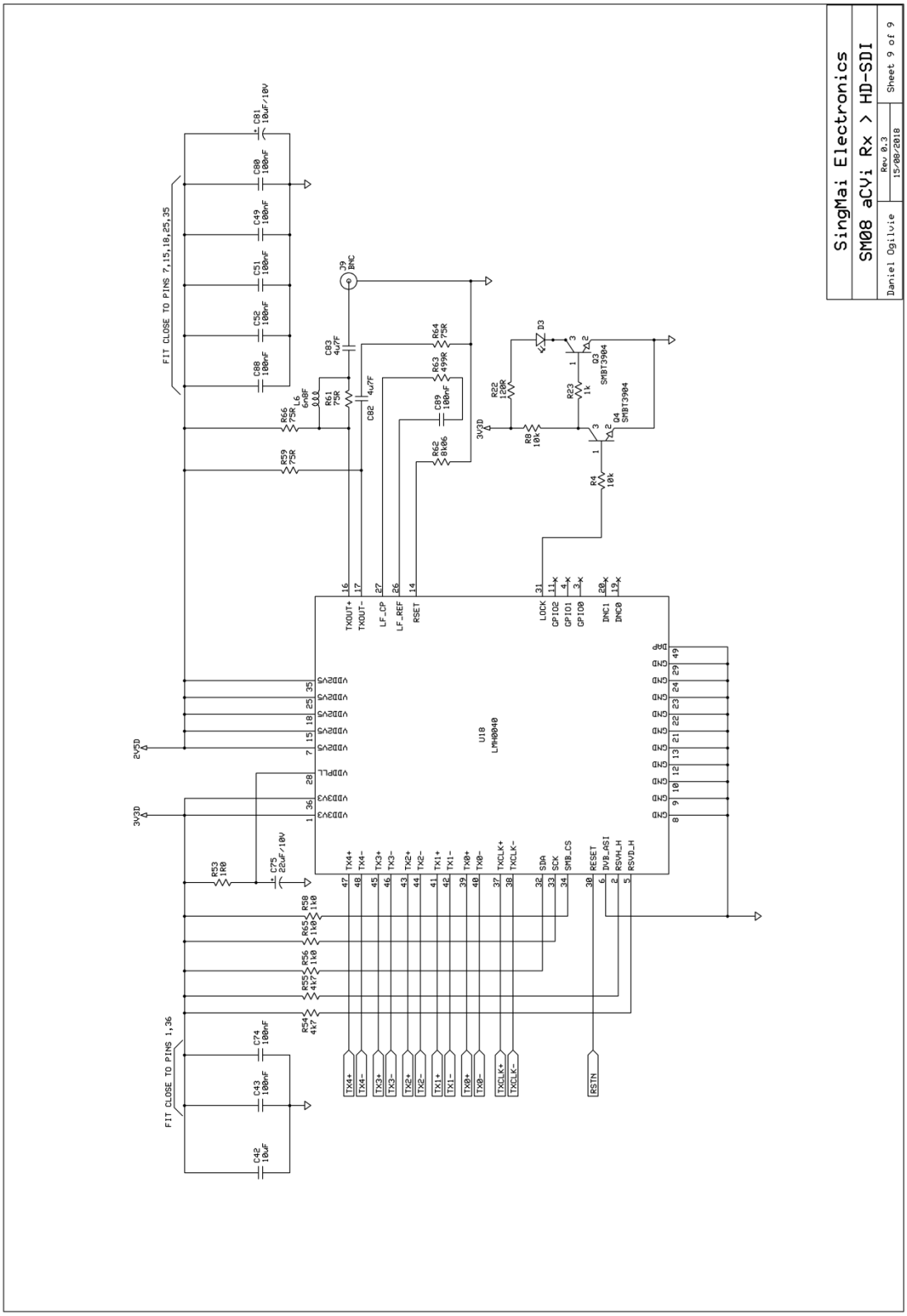


Figure 15 SM08 Schematics - Sheet 9.

5. Specification

Power:	+5VDC ± 5% @ ~450mA.
Dimensions:	120mm x 78mm x 27mm.
HD-SDI output:	SMPTE-292M, 20 bit 4:2:2 YCbCr format.
Video standards:	720p/23Hz, 720p/24Hz, 720p/25Hz, 720p/29Hz, 720p/30Hz, 720p/50Hz, 720p/59Hz, 720p/60Hz, 1080p/23Hz , 1080p/25Hz, 1080p/25Hz, 1080p/29Hz, 1080p/30Hz, 1080i/50Hz, 1080i/59Hz, 1080i/60Hz.
Luma bandwidth:	14MHz ± 1dB. >-50dB @ 17.6MHz.
Chroma bandwidth:	14MHz ± 1dB. >-40dB @ 17.6MHz.
Transmission distance:	>300m of RG-59 coaxial cable. >500m RG-59 cable with reduced luma bandwidth.
Latency:	<100µs (transmitter HD-SDI input to receiver HD-SDI output).
Operating temperature:	-10° to +45°degC.

Appendix A: Power supply specification

The AC-DC converter supplied with the SM06 is a model TE10A0503F01 from SL Power Electronics. It accepts all AC inputs from 90-264VAC and provides a 5V, 2A DC output for the SM06. The detailed specification is shown below.

TE10 Family 10W~12W Single Output External Power Industrial Grade

FEATURES AND BENEFITS

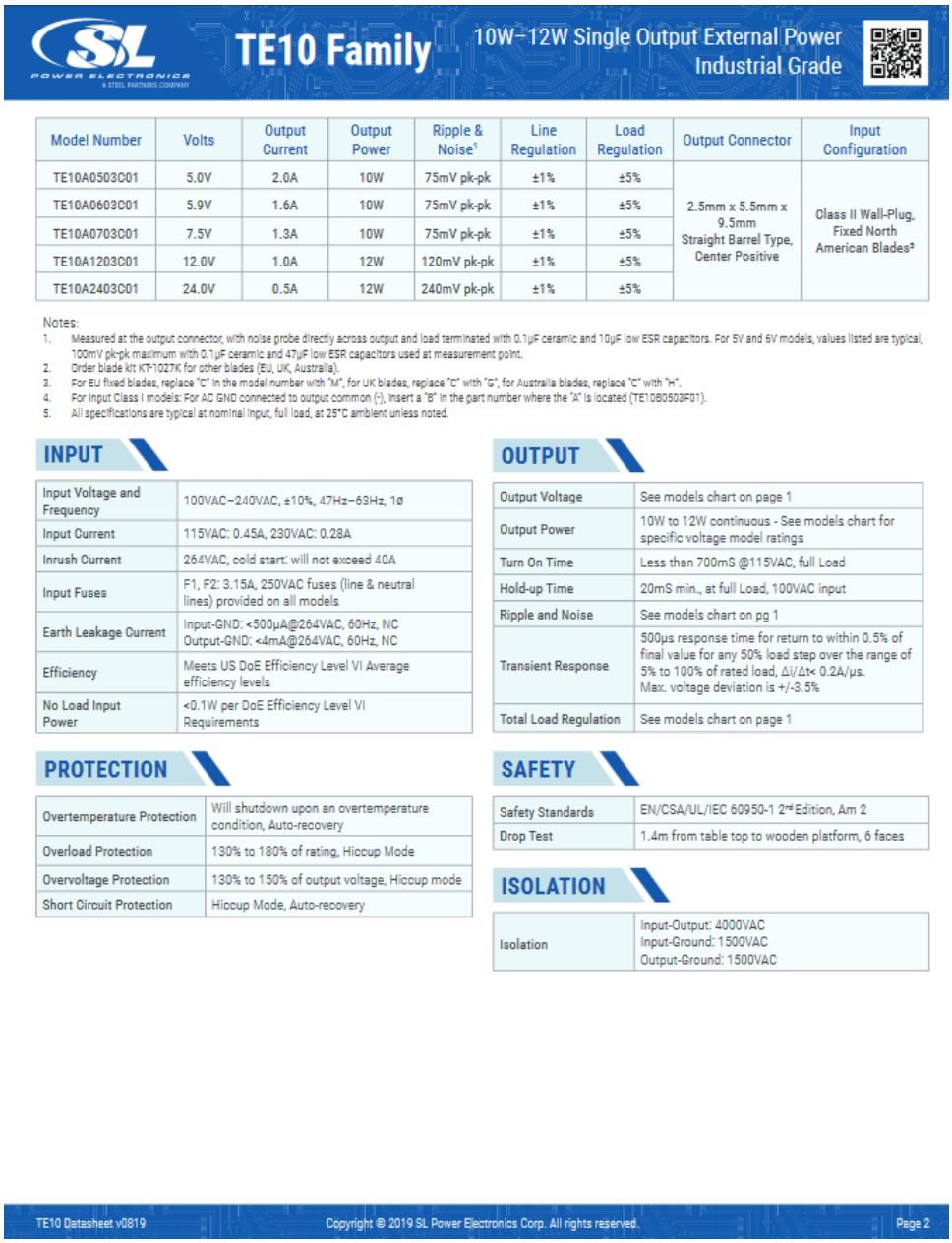
Universal Input 90VAC~264VAC Input Range Desktop and Wall-Plug Versions	Meets "Heavy Industrial" Levels of EN61000 EMC Requirements
Up to 12W of AC-DC Power	>10 Year E-Cap Life
IP22 Rated Enclosure	>1,000,000 Hours MTBF
Approved to EN/IEC/UL60950-1 2nd Edition, Am.2	3 Year Warranty
Meets EN55022/CISPR22, FCC Part 15.109 Class B Conducted & Radiated Emissions, with 6db Margin	Meets DoE Efficiency Level VI Requirements No Load Input Power Average Efficiency

MODEL SELECTION

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503F01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class I Desktop, IEC60320 C14 Receptacle
TE10A0603F01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703F01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203F01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403F01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503N01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C8 Receptacle
TE10A0603N01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703N01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203N01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403N01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503Q01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Desktop, IEC60320 C18 Receptacle
TE10A0603Q01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703Q01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203Q01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403Q01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		
TE10A0503B01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Interchangeable Blades (North American Blade included)[2]
TE10A0603B01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703B01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203B01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403B01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

TE10 Datasheet v0819 Page 1

Figure 16 Power supply specification - page 1.



SL POWER ELECTRONICS
A STEEL PARTNERS COMPANY

TE10 Family

10W–12W Single Output External Power
Industrial Grade

Model Number	Volts	Output Current	Output Power	Ripple & Noise[1]	Line Regulation	Load Regulation	Output Connector	Input Configuration
TE10A0503C01	5.0V	2.0A	10W	75mV pk-pk	±1%	±5%	2.5mm x 5.5mm x 9.5mm Straight Barrel Type, Center Positive	Class II Wall-Plug, Fixed North American Blades[3]
TE10A0603C01	5.9V	1.6A	10W	75mV pk-pk	±1%	±5%		
TE10A0703C01	7.5V	1.3A	10W	75mV pk-pk	±1%	±5%		
TE10A1203C01	12.0V	1.0A	12W	120mV pk-pk	±1%	±5%		
TE10A2403C01	24.0V	0.5A	12W	240mV pk-pk	±1%	±5%		

Notes:
1. Measured at the output connector, with noise probe directly across output and load terminated with 0.1µF ceramic and 10µF low ESR capacitors. For 5V and 6V models, values listed are typical, 100mV pk-pk maximum with 0.1µF ceramic and 47µF low ESR capacitors used at measurement point.
2. Order blade kit KT-1027K for other blades (EU, UK, Australia).
3. For EU fixed blades, replace "C" in the model number with "M", for UK blades, replace "C" with "G", for Australia blades, replace "C" with "H".
4. For Input Class I models: For AC GND connected to output common (-), insert a "B" in the part number where the "A" is located (TE10B0503F01).
5. All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

INPUT

Input Voltage and Frequency	100VAC–240VAC, ±10%, 47Hz–63Hz, 1ø
Input Current	115VAC: 0.45A, 230VAC: 0.28A
Inrush Current	264VAC, cold start: will not exceed 40A
Input Fuses	F1, F2: 3.15A, 250VAC fuses (line & neutral lines) provided on all models
Earth Leakage Current	Input-GND: <500µA@264VAC, 60Hz, NC Output-GND: <4mA@264VAC, 60Hz, NC
Efficiency	Meets US DoE Efficiency Level VI Average efficiency levels
No Load Input Power	<0.1W per DoE Efficiency Level VI Requirements

OUTPUT

Output Voltage	See models chart on page 1
Output Power	10W to 12W continuous - See models chart for specific voltage model ratings
Turn On Time	Less than 700mS @115VAC, full Load
Hold-up Time	20mS min., at full Load, 100VAC input
Ripple and Noise	See models chart on pg 1
Transient Response	500µs response time for return to within 0.5% of final value for any 50% load step over the range of 5% to 100% of rated load, Δi/Δt< 0.2A/µs. Max. voltage deviation is +/-3.5%
Total Load Regulation	See models chart on page 1

PROTECTION

Overtemperature Protection	Will shutdown upon an overtemperature condition, Auto-recovery
Overload Protection	130% to 180% of rating, Hiccup Mode
Overvoltage Protection	130% to 150% of output voltage, Hiccup mode
Short Circuit Protection	Hiccup Mode, Auto-recovery

SAFETY

Safety Standards	EN/CSA/UL/IEC 60950-1 2nd Edition, Am 2
Drop Test	1.4m from table top to wooden platform, 6 faces

ISOLATION

Isolation	Input-Output: 4000VAC Input-Ground: 1500VAC Output-Ground: 1500VAC

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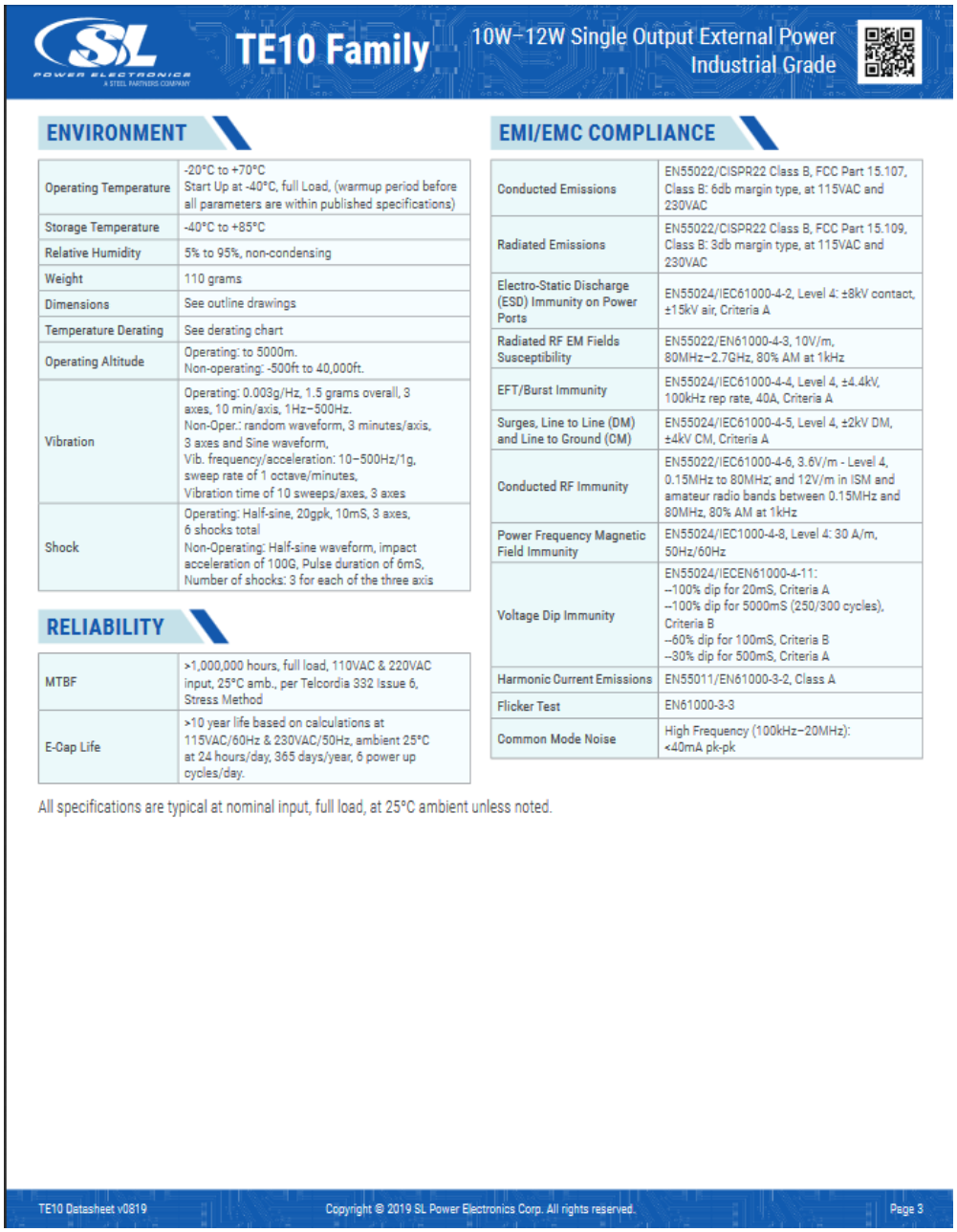
Figure 17 Power supply specification - page 2.



TE10 Family

10W–12W Single Output External Power
Industrial Grade

ENVIRONMENT

Operating Temperature	-20°C to +70°C Start Up at -40°C, full Load, (warmup period before all parameters are within published specifications)
Storage Temperature	-40°C to +85°C
Relative Humidity	5% to 95%, non-condensing
Weight	110 grams
Dimensions	See outline drawings
Temperature Derating	See derating chart
Operating Altitude	Operating: to 5000m. Non-operating: -500ft to 40,000ft.
Vibration	Operating: 0.003g/Hz, 1.5 grams overall, 3 axes, 10 min/axis, 1Hz–500Hz. Non-Oper.: random waveform, 3 minutes/axis, 3 axes and Sine waveform, Vib. frequency/acceleration: 10–500Hz/1g, sweep rate of 1 octave/minutes, Vibration time of 10 sweeps/axes, 3 axes
Shock	Operating: Half-sine, 20gpk, 10mS, 3 axes, 6 shocks total Non-Operating: Half-sine waveform, impact acceleration of 100G, Pulse duration of 6mS, Number of shocks: 3 for each of the three axis

RELIABILITY

MTBF	>1,000,000 hours, full load, 110VAC & 220VAC input, 25°C amb., per Telcordia 332 Issue 6, Stress Method
E-Cap Life	>10 year life based on calculations at 115VAC/60Hz & 230VAC/50Hz, ambient 25°C at 24 hours/day, 365 days/year, 6 power up cycles/day.

EMI/EMC COMPLIANCE

Conducted Emissions	EN55022/CISPR22 Class B, FCC Part 15.107, Class B: 6db margin type, at 115VAC and 230VAC
Radiated Emissions	EN55022/CISPR22 Class B, FCC Part 15.109, Class B: 3db margin type, at 115VAC and 230VAC
Electro-Static Discharge (ESD) Immunity on Power Ports	EN55024/IEC61000-4-2, Level 4: ±8kV contact, ±15kV air, Criteria A
Radiated RF EM Fields Susceptibility	EN55022/EN61000-4-3, 10V/m, 80MHz–2.7GHz, 80% AM at 1kHz
EFT/Burst Immunity	EN55024/IEC61000-4-4, Level 4, ±4.4kV, 100kHz rep rate, 40A, Criteria A
Surges, Line to Line (DM) and Line to Ground (CM)	EN55024/IEC61000-4-5, Level 4, ±2kV DM, ±4kV CM, Criteria A
Conducted RF Immunity	EN55022/IEC61000-4-6, 3.6V/m - Level 4, 0.15MHz to 80MHz; and 12V/m in ISM and amateur radio bands between 0.15MHz and 80MHz, 80% AM at 1kHz
Power Frequency Magnetic Field Immunity	EN55024/IEC1000-4-8, Level 4: 30 A/m, 50Hz/60Hz
Voltage Dip Immunity	EN55024/IECEN61000-4-11: –100% dip for 20mS, Criteria A –100% dip for 5000mS (250/300 cycles), Criteria B –60% dip for 100mS, Criteria B –30% dip for 500mS, Criteria A
Harmonic Current Emissions	EN55011/EN61000-3-2, Class A
Flicker Test	EN61000-3-3
Common Mode Noise	High Frequency (100kHz–20MHz): <40mA pk-pk

All specifications are typical at nominal input, full load, at 25°C ambient unless noted.

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Figure 18 Power supply specification - page 3.